THOMSON CONSUMER ELECTRONICS INC./TECHNICAL TRAINING/P.O. BOX 1976 INDIANAPOLIS IN 46206

The CTC 168/169

Technical Training Manual

RCA

Color Television Receivers

FOREWORD

This Technical Training manual familiarizes service technicians with the circuits used in RCA and GE Brand color televisions using the CTC168/169 chassis. This manual contains circuit descriptions and service procedures developed to aid the service technician during troubleshooting and servicing CTC168/169 television receivers. This manual also contains information on general troubleshooting techniques and several appendices. The appendices include: a frequency and bandswitch state chart, microcomputer pin designations and in-circuit resistance measurements for the color television processing IC U1001.

Note: This publication is intended to be used only as a training aid. It is not intended to replace service data. RCA and GE Service Data for these instruments contains specific information about parts, safety, and alignment procedures and must be consulted before performing any service.

SAFETY INFORMATION CAUTION

Safety information is contained in the appropriate RCA or GE Service Data. All product safety requirements and testing must be complied with prior to returning the intrument to the consumer. Servicers who defeat safety features or fail to perform safety checks may be liable for any resulting damages, and may expose themselves and others to possible injury.

All integrated circuits, all surface mounted devices, and many other semiconductors are electrostatically sensitive and therefore require special handling techniques.

Prepared by
Thomson Consumer Electronics, Inc.
Technical Training
PO Box 1976
Indianapolis, Indiana 46206

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INTRODUCTION

The CTC168 and CTC169 color television chassis are the latest additions to the RCA and GE brand Unitized Chassis family. While much of the technology employed in the current chassis family is retained in the CTC168 and CTC169, the circuit configurations have changed dramatically. In addition, the CTC169 chassis is used in both direct view and projection television receivers.

Chassis Variations

The CTC168 chassis is used in models with 20″ picture tubes. The CTC169 chassis is used in 27″, 31″, and 35″ direct view receivers and also in projection receivers. The basic chassis is modified by changing SIP boards to provide a wide range of features. The chassis can be used from middle of the line models to high end models. The CTC168 and CTC169 chassis vary mainly in the deflection circuits to compensate for the various screen sizes.

There are four models of projection receivers which use the CTC169 chassis. Three of the models have a 46″ screen and the fourth has a 52″ screen. Two of the models are equipped with a pix-in-pix feature. There is very little difference between the chassis used in the projection receiver and the chassis used in the direct view models. The major differences are covered in the projection television portion of the manual.

New Features

There are a number of new features available in the CTC168/169 chassis. The features are covered in more detail in the system control portion of the manual, since the majority of the features depend on the system control microcomputer to function. The new features include:

- Pix-in-Pix
- Digital Comb Filter
- White Stretch and Black Stretch Circuits
- Channel Labeling
- Auto VCR Input Select
- Commercial Skip
- Universal Remote Control

The pix-in-pix module is not as highly featured as the CPIP module used in the CTC140 chassis. The module provides picture in picture and picture swap but does not have the zoom feature of CPIP. The receivers which have the digital comb filter also have the white stretch and black stretch circuits. The comb filter removes chroma noise from luminance signal. The white and black stretch circuits improve the perceived contrast in the picture. The white stretch circuit operates in low brightness scenes and affects the white portion of the picture content. The black stretch circuit operates in high brightness scenes and pulls the low level portion of the picture to black.

Channel labeling allows the user to add up to 4 characters per channel and a total of 40 labels. The remote hand unit is used to create or erase labels. The commercial skip feature places a timer display on the screen. The channel can be changed while the timer is displayed. When the timer reaches zero, the channel is switched back to the original station. Each time the channel skip button is pressed the timer is increased in 30-second steps. The timer can be set for a maximum of four minutes. Pressing the clear button on the hand unit cancels the channel skip command.

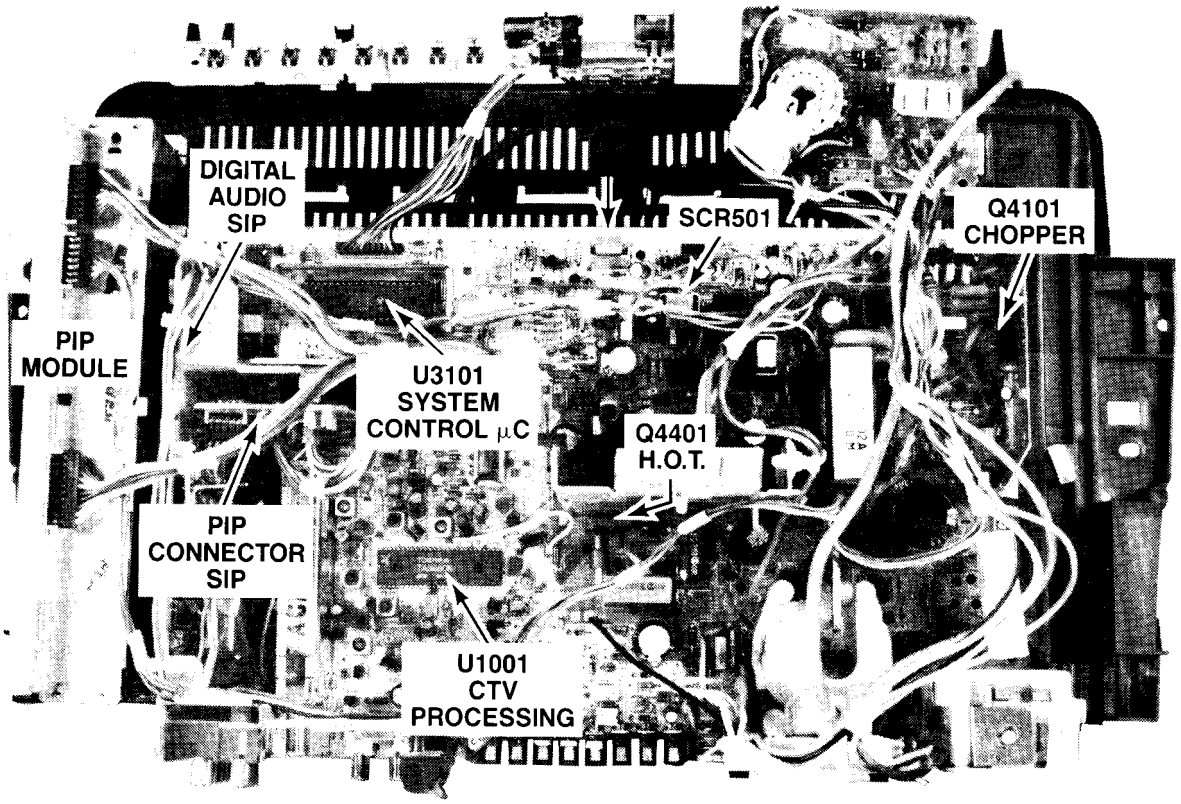
The Auto VCR input select feature automatically changes the channel to the selected video input when the VCR1 button on the hand unit is pressed. The selected channel can be any of the video inputs or any RF channel. The VCR channel setup is located on the setup menu.

The universal remote control hand unit will control the television, two compatible VCRs, and a cable converter box. There are a number of different brands which can be controlled with this hand unit. The codes are periodically updated when new information is received concerning additional models and brands of VCR and cable converter/descrambler units is received.

New Circuit Areas

The CTC168/169 chassis has a number of new circuits. Most of the changes are refinements of circuits used in previous chassis, but some are new circuits which perform the same functions in different ways. The new areas include:

- Switching Regulator – The use of a switching regulator is not new. However, the regulator used in the CTC168/169 provides both the standby and run supplies for the chassis. There is no standby transformer.
- Vertical – The vertical circuit is similar to a switching power supply. A horizontal rate signal is used to provide the power for the vertical deflection. The scan is controlled by an SCR.
- Tuner – The tuner has changed to include the band-switching and tuning voltage generation. The inputs to the tuner are the B+ supply and clock and data inputs from the system control microcomputer.
- System Control Microcomputer – The functions of the system control microcomputer and the AIU have been combined into one integrated circuit. The system control microcomputer has a communications bus to send commands to the tuner, the digital audio circuit, the digital comb filter, and the EEPROM. It also provides control signals to the color television processing IC U1001.
- Digital Audio – The MTS decoder is now a digital IC with fewer adjustments than previous designs.
- Digital Comb Filter – The digital comb filter removes chroma noise from the luminance signal.



CTC169 Chassis

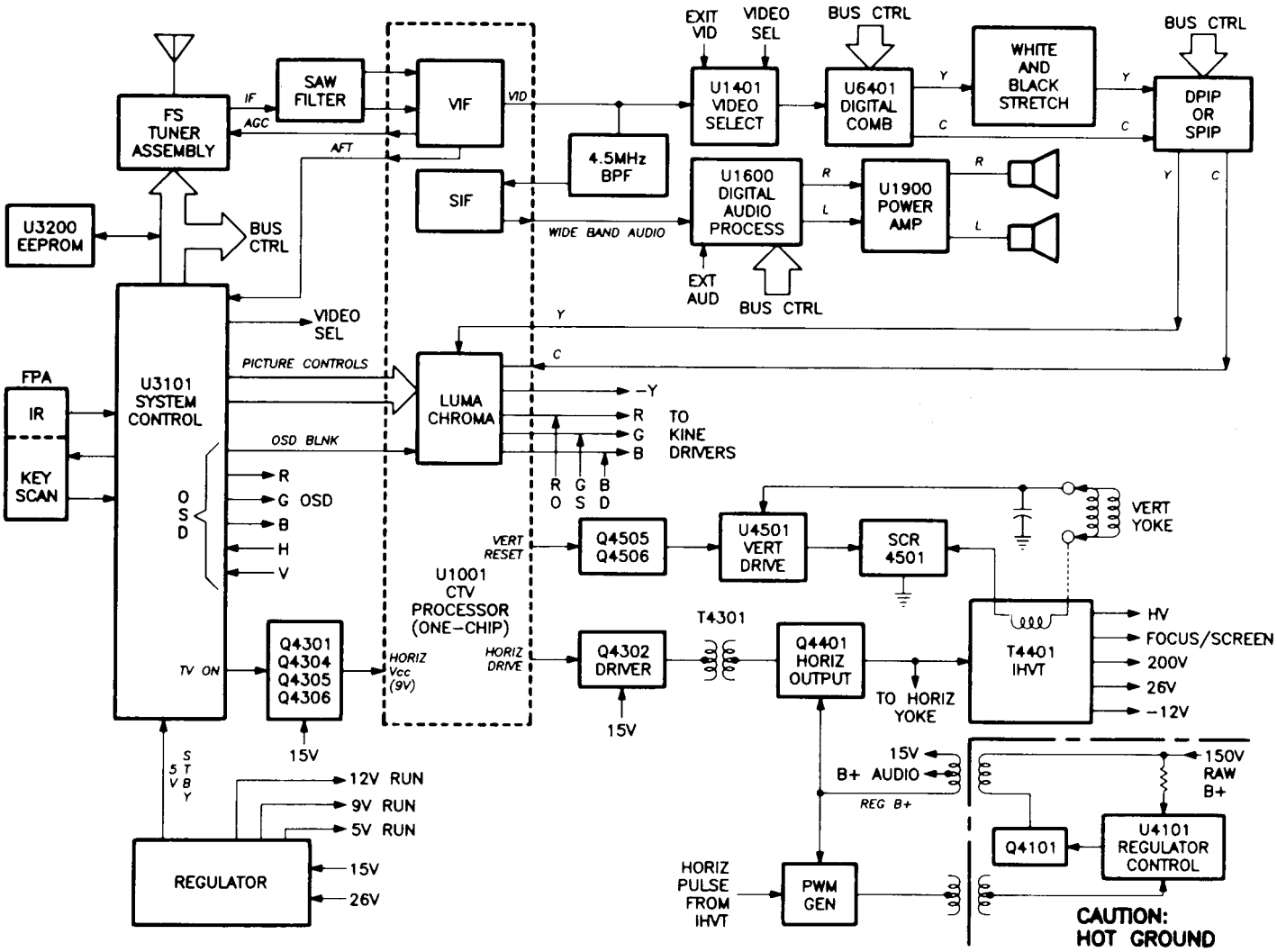


Fig. 1 CTC168/169 Block Diagram

The CTC168/169 chassis can be divided into five major circuit areas. These major functional areas are:

- Power Supply
- System Control/Tuning
- Signal Processing
- Audio
- Deflection

Power Supply

The power supply is a chopper type switching regulator which supplies both the standby and run B+ supplies. Q4101 is controlled by the regulator IC to provide the Reg B+, 15V supply, and B+ for the audio output amplifier. The 15V supply is routed to a regulator to develop the 5V standby supply. The 5V standby supply keeps the system control microcomputer operational whenever AC power is applied. The 5V standby supply is also routed to the front panel assembly for the remote receiver and the keyboard scan circuits.

In the standby mode, the audio circuit is off, so there is no load on the audio B+ line. The reg B+ also has no load since the horizontal deflection circuit is not operating. The 15V supply is routed to the horizontal driver stage to provide power to the driver stage. The regulator uses a different regulation system mode than it uses in the run mode.

The chassis is turned on by the system control microcomputer. The microcomputer biases a switching transistor on to supply power to the horizontal section of U1001. When the horizontal circuit begins to operate, the scan derived 26V supply is generated. The 26V supply is used by the regulator as a bias supply for the run power supplies. If the horizontal circuit fails to operate, none of the run B+ supplies will be present.

When the chassis is operational, the regulator circuit uses a pulse width modulated feedback signal to control the reg B+ supply. The PWM generator samples the level of the reg B+ supply and uses horizontal rate pulses to develop the control signal. The control signal is transformer coupled to the regulator control IC. The regulator control circuit is referenced to hot ground while the remainder of the chassis is reference to cold ground.

System Control
Unlike the CTC156/159 chassis which used a system control micro and an analog interface unit (AIU), the CTC168/169 chassis contain one microcomputer U3101 to perform the system control functions. U3101 contains a serial communications bus which transmits commands and data to peripheral circuits within the chassis. Devices under bus control are the tuner, digital audio IC, digital comb filter, Pix-in-Pix module, and an optional EEPROM.

The system control micro also receives IR remote commands from the IR receiver and scans the keyboard on the front panel assembly (FPA). On-screen display characters are generated by U3101 and applied to the CRT driver stages to produce characters on the screen. U3101 receives horizontal and vertical signals from the chassis for OSD timing.

U3101 generates pulse width modulated (PWM) signals which are filtered to provide DC control voltages for the picture controls such as color, tint, brightness, sharpness, and contrast. Video selection control lines from U3101 are applied to the video input selection circuit to select between the TV tuner or an external video input for viewing on the screen.

There are no configuration code pins on the system control micro to select various feature options as in past chassis. Feature options are stored in the optional EEPROM U3200. U3200 provides nonvolatile memory storage for channel scan lists, convergence settings (projection only), channel label information, and digital comb filter setup parameters.

Signal Processing
The IF signal from the tuner is processed in the CTV processor U1001 (one-chip) to produce the composite video signal which is applied to the video selection stage. The RF AGC voltage is developed in the one chip to control the gain of the tuner. The AFT voltage is also developed in U1001 and applied to the system control micro for use during tuning operations.

The video input selection stage selects between the internal tuner video source or from the external video inputs on the back of the set. The selected video source is applied to either an analog or digital comb filter.

Sets with digital comb filters also contain the white and black stretch circuits sometimes referred to as automatic gamma correction. The white stretch stage boosts the whites in low average picture level (APL) scenes while the black stretch circuit stretches the blacks in high APL scenes to enhance the contrast between black and white picture content.

Some sets contain a DPIP or SPIP module to create the Pix-in-Pix feature. The DPIP module only produces the small pix on the screen while the SPIP module contains multiple features such as big pix freeze, zoom, and multichannel mode. The Y and C outputs of the PIP module is applied to the one-chip to produce the RGB and -Y signals used to drive the CRT.

Audio Processing
The 4.5 MHz band pass filter removes the audio IF signal from the video signal for application to the sound IF stages within U1001. The wide band audio output of the one chip is applied to the digital audio processing IC U1600. This IC is used for MTS/SAP decoding, audio source selection, volume/mute/tone/balance control, and expanded stereo operation. The IC receives its operational commands through the serial communications bus from the system control micro U3101.

The right and left audio signals from U1600 are applied to the audio power amp to drive the speakers. Direct view sets contain either a 1 or 5 watt per channel power amp while projection sets contain a 10 watt per channel amp.

Deflection
The horizontal deflection circuit is similar to many recent chassis. U1001 supplies the horizontal drive signal. The horizontal drive pulse is routed to the base of the horizontal driver transistor. The output of the horizontal driver is transformer coupled to the base of the horizontal output transistor. The horizontal output transistor drives both the primary of the high voltage transformer and the horizontal yoke. U1001 also contains the X-ray protection circuit.

The vertical circuit uses an output from U1001 to reset the ramp generator. The ramp generator provides a reference ramp to the vertical drive IC. The vertical drive IC generates the gate drive signals for the SCR. The winding in the high voltage transformer provides the power for the vertical scan. The capacitor at the top of the vertical yoke winding is charged during horizontal retrace. The SCR is used to vary charge on the capacitor in order to scan the beam down the face of the CRT.

B+ REGULATOR OPERATION

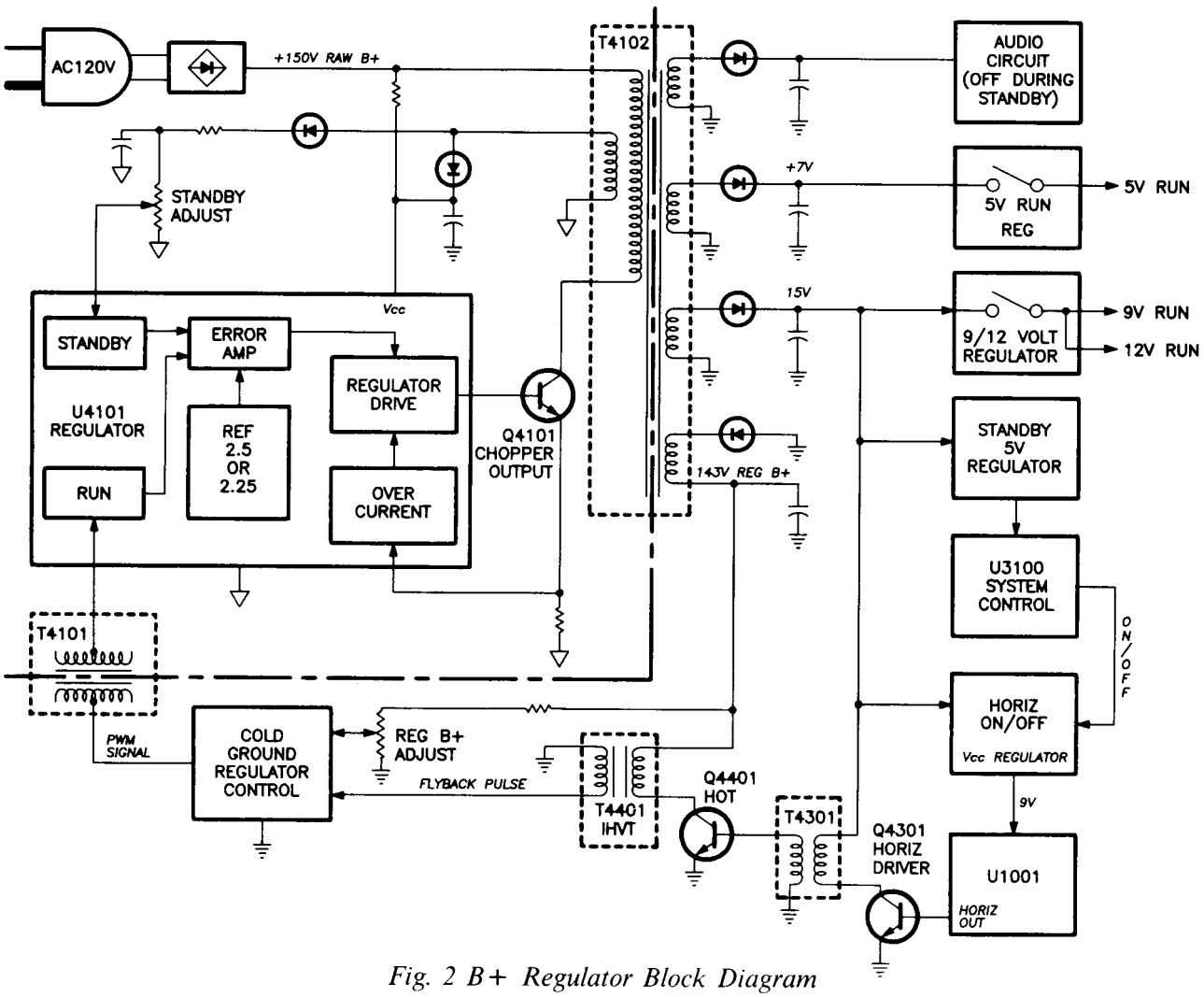


Fig. 2 B+ Regulator Block Diagram

B+ Regulator Overview

The B+ regulator provides both the standby and run power supplies. The regulator is a switched mode supply which operates whenever AC power is applied. The supplies developed by the secondary of the transformer are all switched off in the standby mode to reduce the power consumption when the set is off.

The regulator control IC has two different regulation modes. In the standby mode, a sample from the hot ground side of the regulator provides a DC input to the error amplifier in the regulator control IC. In the run mode, a pulse width modulated signal is transformer coupled to the regulator control IC. The PWM signal is developed from the reg B+ supply and a pulse from the high voltage transformer. The output of the regulator control IC drives the chopper output transistor. By controlling how long the output transistor is conducting, the amount of energy transferred to the secondary is controlled.

Standby Operation

The 120V AC input is rectified to become the 150V raw B+. The raw B+ is routed through the output transformer to the collector of the chopper output transistor. The raw B+ is also passed through a dropping resistor to provide the startup supply for the regulator control IC. In the standby mode, the regulator control IC develops series of output pulses. The pulses are produced at a 20kHz rate, but are not continuous. The internal reference voltage is switched from 2.5 volts to 2.25 volts to provide a reference voltage for the error amplifier. The reference voltage is 2.5 volts when the regulator is producing output pulses and 2.25 volts when production of the output pulses is inhibited. The switching occurs when the regulator output reaches the minimum duty cycle. While the reference voltage is 2.5V, the IC produces drive pulses until the feedback voltage reaches 2.5V. The reference voltage is then switched to 2.25V. No pulses are generated until the feedback voltage drops below 2.25V.

The regulator IC turns on when the input voltage at the Vcc input rises above ten volts. The IC remains on until the voltage drops below 7.5 volts. The raw B+ input is only used to start the IC. Once output pulses are generated, a winding in the output transformer is used to supply both the power to the regulator IC and the feedback signal to the error amplifier. The pulses from the run winding are rectified and filtered before being routed to the IC as a DC voltage. The standby adjust control is used to set the level of the reg B+ supply. A separate feedback loop and adjustment control the output of the regulator in the run mode. The standby 5V supply is the only supply used in the standby mode. The other outputs of the switching regulator are present, but the circuits are disabled to reduce the power consumption during standby. The reg B+ supply is present, but since the horizontal circuit is not operating in the standby mode, the load on the supply is minimal. In the standby mode, the reg B+ supply is approximately 140 volts. The supply provides 143 volts when the set is on.

On/Off Operation

The 5 volt standby supply is routed to the microcomputer when the set is off. The system control microcomputer must remain operational in order to detect when a front panel key is pressed or when a remote command is received. Power must also be supplied to the horizontal driver and horizontal output stages. This enables the horizontal circuit to become operational when the power button is pressed. The on/off operation is similar to previous chassis where the color TV processing IC is used, that is, the chassis is turned on by supplying power to the horizontal oscillator. When the horizontal circuit is operational, the scan-derived supplies provide the power to the remainder of the chassis.

When the power button is pressed, the system control microcomputer detects the key press and sends the TV ON signal to an on/off switch transistor. When the on/off switch is turned on, the B+ regulator for the horizontal portion of U1001 is enabled. U1001 develops a horizontal drive pulse. Since the horizontal driver and the horizontal output transistors have B+ applied to their collectors, they turn on when the drive pulse is present. Once the horizontal circuit is operational, the scan derived supplies are used to turn on the 5-volt run regulator and the 9/12-volt run regulator, supplying power to the remainder of the chassis. When the set is turned off, the power to the horizontal oscillator is removed, causing the horizontal circuit to cease operation.

Run Mode

In the run mode the load on the switching power supply increases. The chopper output transistor is turned on longer to provide the additional power to the secondary supplies. The regulator changes modes of operation to handle the increased load. The internal reference voltage of the regulator IC is switched from 2.25 volts to 2.5 volts. The feedback signal is provided by a pulse width modulator rather than from the resistor divider used in the standby mode. The pulse width modulator uses both a resistor divider connected to the reg B+ supply and a horizontal rate pulse supplied by the high voltage transformer to develop the control signal for the regulator IC. The cold ground regulator control circuit provides better regulation than the standby mode control circuit. The on time of the pulse width modulated signal varies with the reg B+ level in order to change the duty cycle of the chopper output transistor. During the run mode, the chopper runs at a horizontal rate.

The regulator control IC has an overcurrent shutdown circuit. A resistor in the emitter circuit of the chopper output transistor provides a voltage which is proportional to the current through the chopper transistor. When the current exceeds the threshold level, the overcurrent circuit disables the regulator drive pulses. If the cause of the overcurrent condition remains, the overcurrent circuit again disables the regulator output.

Troubleshooting Overview

When troubleshooting the B+ regulator circuit, it is necessary to remember that there are two distinct modes of operation. The switching regulator is used to provide both the standby and run supplies. If the standby operation is incorrect, the run mode can not be checked. If the cold ground regulator control circuit fails to operate, the regulator tries to provide the proper outputs using the standby control circuit, however the regulator can not respond quickly enough. The set will operate, but the picture size will change depending on the scene content.

Most problems in the switching regulator circuit will result in a dead set symptom. If the fuse is blown suspect a shorted chopper output transistor.

If the standby supplies are present, a dead set symptom could still be caused by either the on/off circuit and system control microcomputer, or the horizontal deflection circuit.

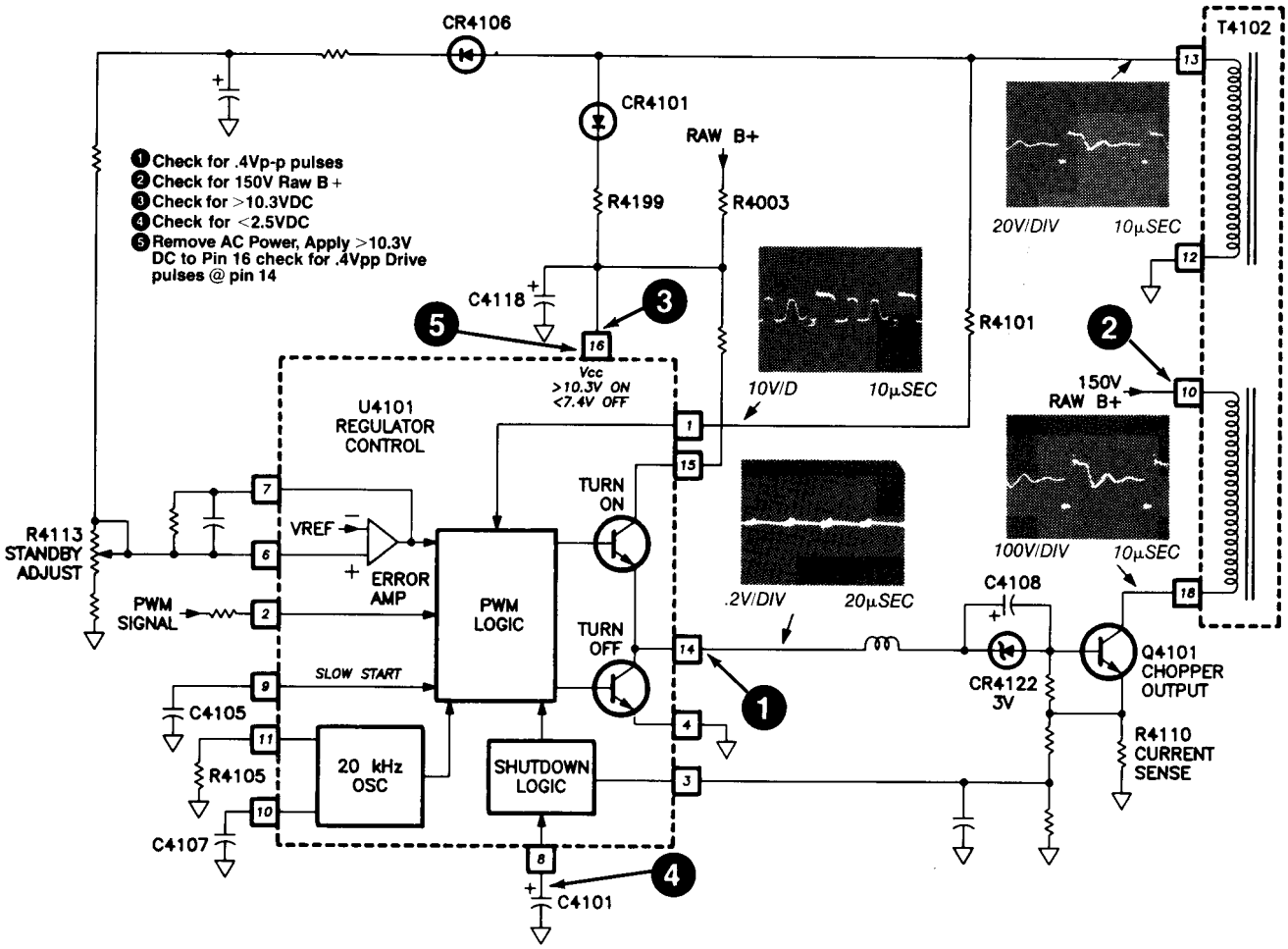


Fig. 3 B+ Regulator Standby Circuit

B+ Regulator Standby Circuit Operation

The switching regulator circuit is used to provide the standby supplies, taking the place of the standby transformer. In order to reduce the power consumption of the set in the standby mode, the switching regulator has two different modes of operation. In the standby mode, the output transistor is turned on for a series of pulses and then remains off. The power demand in the standby mode is small, so the short on time is sufficient to provide all the standby supplies. The regulator uses a feedback winding in the output transformer to provide the B+ for the regulator control IC and the feedback signal for the error amplifier. The circuit does not provide tight regulation of the standby supplies but the regulation of the standby supplies is not critical. In the run mode, the regulator control IC provides a horizontal-rate pulse-width modulated drive signal. The cold ground control circuit enables the regulator to control the reg B+ much more closely than in the standby mode.

Since the regulator provides the standby supplies, the regulator circuit operates whenever AC power is applied. The raw B+ is routed through R4003 and begins to charge C4118. The regulator control IC turns on when the voltage at pin 16 rises above 10.3 volts. (The regulator circuit continues to operate until the voltage drops below 7.4 volts). The regulator control IC contains a 20kHz oscillator. The oscillator free runs at 20kHz. If the power supply does not start, the IC turns off, allowing C4118 to charge to 10.3V.

The slow start capacitor C4105 limits the on time of the chopper output transistor during the first few cycles to prevent over-stressing the output device. CR4122 and C4108 in the base circuit of the chopper output transistor are a waveshaping network to produce the proper turn on and turn off signal for the chopper output transistor. The regulator control IC output stage contains both a turn on and a turn off transistor. The turn on stage provides the base current for the chopper transistor. The turn off stage ensures that the base drive is removed to provide a faster turn off time for the chopper.

When the chopper output transistor is turned on, current flows through the primary of T4102. A voltage is induced in a secondary winding of the transformer when the chopper turns off. This voltage is rectified by CR4101 and supplies the run B+ for the regulator IC. R4199 limits the peak voltage spikes applied to the Vcc input of the IC. The IC will shutdown if the input voltage exceeds 15 volts. A second rectifier, CR4106, provides the feedback signal to the error amplifier. The DC voltage is routed through R4113, the standby adjust potentiometer. R4113 sets the level of the feedback signal applied to the error amplifier in the regulator IC. The feedback signal is compared to a fixed reference signal. The difference between the feedback signal and the reference signal enables the logic circuit to determine if the output voltage is too high or too low.

The voltage from the secondary winding is also used by the logic circuit in U4101 to determine when to turn the output transistor on. The output transistor is not turned on until the transfer of energy in the transformer is complete. The voltage at pin 1 is both positive and negative with respect to ground. The output stage can not be turned on while the voltage at pin 1 is above ground. The logic circuit checks the input at pin 1 when changing from the standby mode to the run mode and vice versa.

When the regulator is operating, the current through R4110 is monitored to detect an overcurrent condition. The voltage at the emitter of Q4101 is proportional to the current through the transistor. The pulses through the transistor are integrated and applied to pin 3 of the regulator IC. If the voltage at pin 3 exceeds 0.6 volts, the overcurrent circuit is activated. There are two different overcurrent modes. If the voltage at pin 3 is above 0.6 volts but less than 0.9 volts, the overcurrent circuit temporarily halts the output of the regulator IC. If the voltage at the input pin is greater than 0.9 volts, the regulator IC turns off and will not restart until the AC power is removed or the B+ supply to the IC drops below 5 volts. In this second shutdown mode, the voltage at the B+ input pin varies just as if the IC was trying to start.

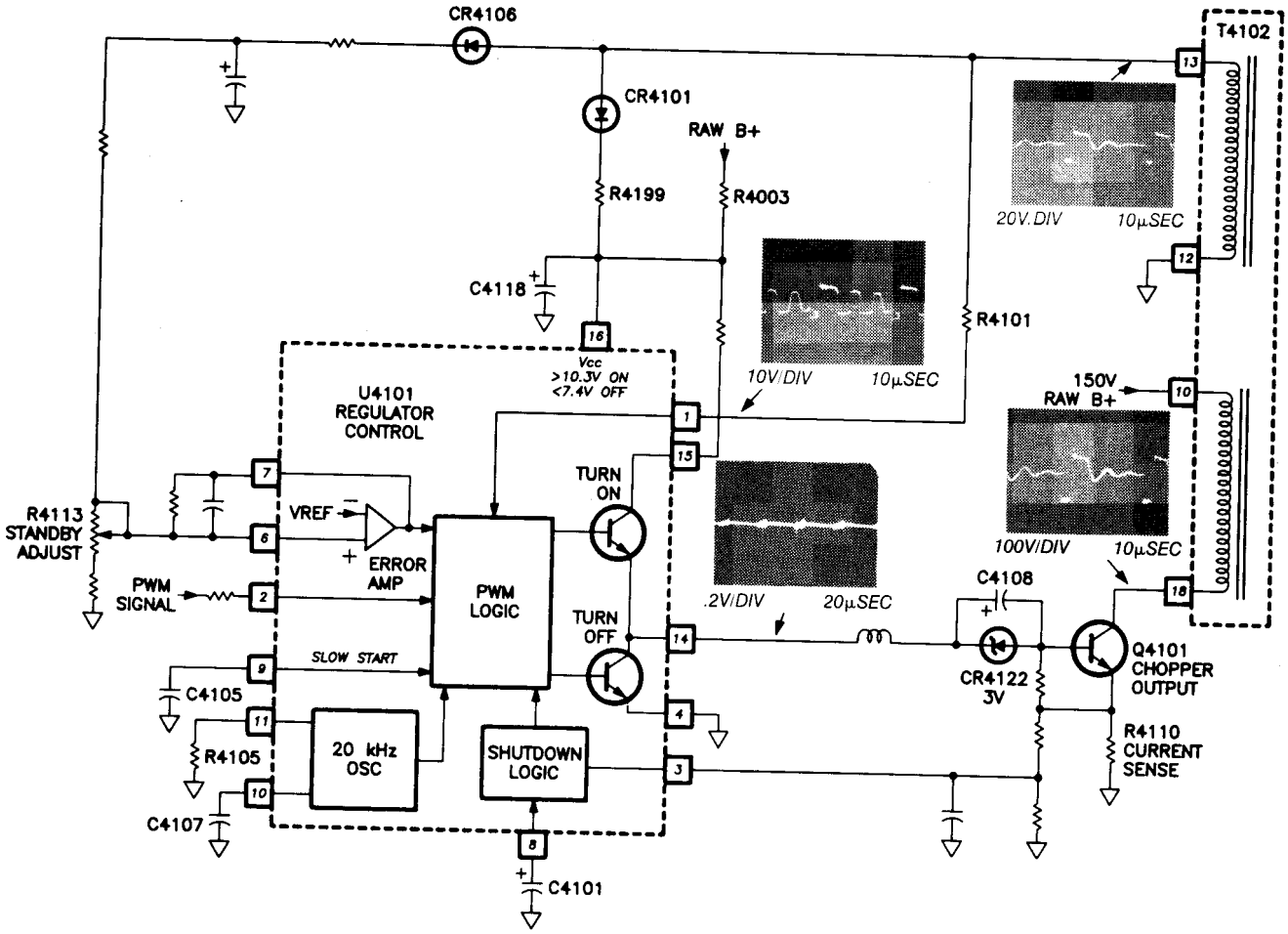


Fig. 3 B+ Regulator Standby Circuit (repeated)

Troubleshooting Strategies

Dead Set

A dead set symptom can be caused by any of the five major circuit areas. For example, in any receiver with the ten-watt-per channel audio system, a malfunction in the audio can cause the system control microcomputer to cycle on and off. Malfunctions in the digital comb filter can cause the microcomputer to lock up, again giving a dead set symptom. Problems in the microcomputer will give a dead set symptom and any malfunctions in the horizontal deflection circuit produce a similar result. Finally, most problems in the chopper power supply also produce a dead set symptom. A quick check of the chopper power supply operation is to check the standby 15 volt supply. If this supply is present, the power supply is probably operating normally and the problem is located elsewhere on the chassis.

Standby Supply Missing

If the standby supplies are missing, first check the raw B+ input, line fuse, and surge resistor.

- Raw B+ Missing – If the raw B+ is missing at the collector of the chopper output transistor, the line fuse or the surge resistor is probably open. The usual cause is a shorted chopper output transistor. If the chopper transistor is open, it is necessary to check the current sense resistor before restoring power to the set. In addition, it is necessary to check the resistance of the secondaries of T4102 to try to determine the cause of the failure. The resistance to ground from the cathode of all the secondary supplies except the fifteen volt line should be greater than 100k ohms. The resistance from the cathode of CR4118 to ground should be greater than 4k ohms. If any resistance measurement is less than this, correct the problem on that supply before restoring power to the set. If the chopper output transistor is shorted, the IC could also be damaged. After the transistor is replaced, measure the voltage at U4101-16. If the voltage is less than 2.5V, the IC is shorted. If the voltage bounces between 7 and 10 volts, suspect overcurrent shutdown.
- Raw B+ is Present – If the raw B+ is present at the collector of the chopper output device but the standby supplies are missing, the problem could be overcurrent shutdown, overvoltage shutdown, or a malfunction in the regulator control IC and associated components.

1. Measure the DC voltage to hot ground at pin 8 of U4101. If the voltage is greater than 2.5 volts, the IC is in the overcurrent shutdown mode.
2. If the voltage at pin 16 is greater than 10.5 volts and less than 15 volts, the IC should begin operation. An overcurrent condition could exist which does not cause the IC to latch off. Using an oscilloscope, measure the p-p voltage at U4101 pin 3. The voltage is less than 0.6 volts during normal operation. If the voltage is between 0.6 and 0.9 volts, the regulator cycles on and off. If the voltage is greater than 0.9 volts, the IC latches off until AC power is removed.

Overcurrent Shutdown
An overcurrent shutdown condition is normally caused by a shorted or leaky component on one of the secondary supplies. For example, a shorted horizontal output transistor or "S" shaping capacitor causes an overcurrent condition. Check the resistance of the secondaries of the transformer to determine which supply is defective. See the section on raw B+ missing for the proper resistance measurements.

Overvoltage Shutdown
U4101 enters an overvoltage shutdown mode if the input Vcc rises above 15.7 volts. The IC stays off until AC power is removed. Overvoltage conditions can be caused by an open in the standby adjust voltage input to the error amplifier or a spike on the Vcc line due to insufficient filtering. Remove AC power and discharge C4118. Verify the components in the feedback input to the error amplifier. Restore AC power and check for normal operation. An overvoltage condition can occur if the cold side B+ regulator was regulating at too high a voltage or if C4118 becomes leaky.

No Output from U4101
If there is no output from U4101 and there is no overcurrent or overvoltage condition, use an external DC power supply to confirm operation of the IC. Remove AC power and connect a DC supply to pin 16 of U4101. Monitor the output of the IC at pin 14. Raise the DC input above 10.5 volts and check for an output waveform. If the output is present, check for base drive directly on the base of the chopper transistor.

If the output pulses are missing at pin 14 of U4101, check for the 20kHz clock signal at pins 10 and 11. If the signal is missing, suspect C4107, R4105, or U4101.

If the IC operates normally when using an external DC supply but does not operate when AC power is applied, check the voltage at pin 3 for an overcurrent shutdown condition. The IC latches off if the peak voltage input at pin 3 rises above 0.9 volts. Measure the Vcc input. The voltage at pin 16 must rise above 10.5 volts before the IC will begin operation. Once the IC turns on, the voltage at pin 16 can drop as low as 7.5 volts before the IC shuts off. If the input voltage is too low, suspect a leaky C4118. If the Vcc input is greater than 10.5 volts and there is no overcurrent condition, but the IC still does not produce an output, suspect a defective U4101.

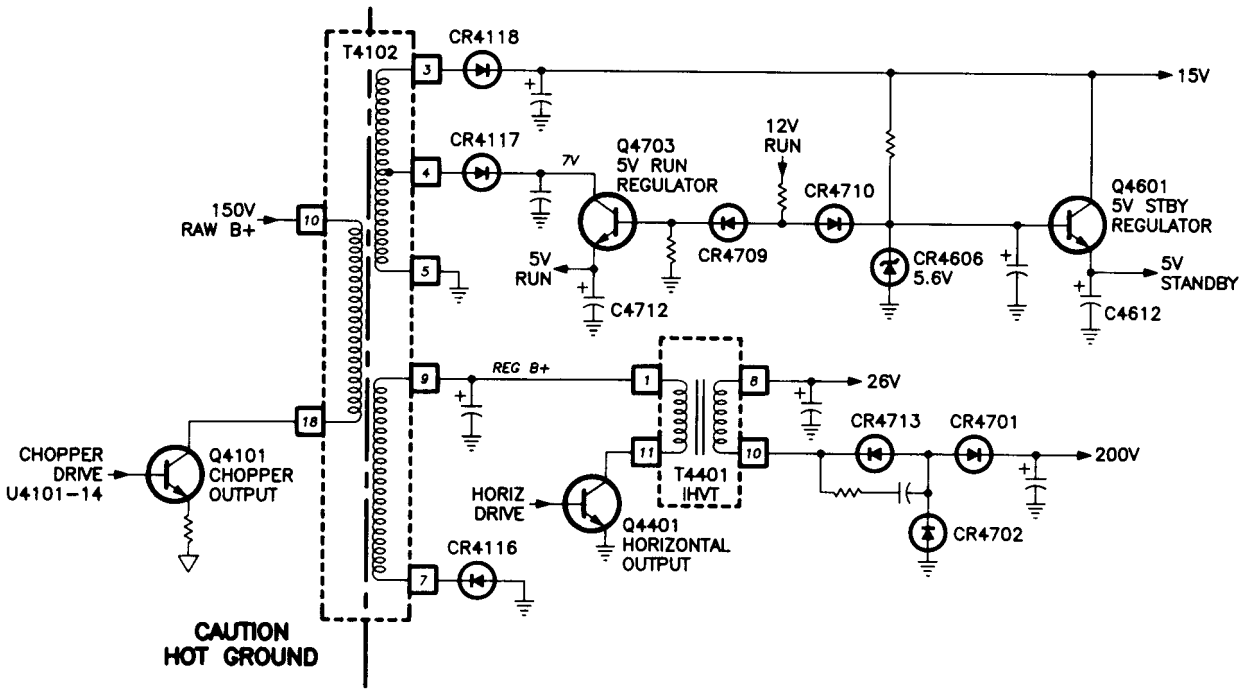


Fig. 4 Standby Power Supply Circuit

Standby Power Supply Operation

The standby power supply circuit provides the power supplies needed by the chassis to detect when the power on command is received and to enable the chassis to begin operation. The system control microcomputer is on whenever AC power is applied. The system control microcomputer scans the front panel keys to detect when the power button has been pressed. The system control microcomputer also receives the input from the IR receiver to determine when the remote on command was issued. The reg B+ supply is present to enable the horizontal circuit to begin operation quickly. The remainder of the chassis receives power after the horizontal circuit begins operation.

When the chopper output transistor is turned on by the regulator IC, current flows through the primary of the transformer. Energy is transferred to the secondary of the transformer. The pulses are rectified and filtered to become the standby supplies for the chassis.

The 15-volt supply provides the input to the 5-volt standby regulator. The 15-volt supply is also routed to the horizontal driver transformer. Since the horizontal circuit is turned off in the standby mode, there is only a small load on the 15-volt supply. The 5-volt standby supply is developed by Q4601, the 5-volt standby regulator transistor. CR4606 in the base circuit of Q4601, provides a 5.6V reference level at the base. The voltage at the emitter of Q4601 is approximately one diode drop below the base voltage.

The 5-volt run regulator, Q4703, is off in the standby mode. The 12-volt run supply is not present until the scan-derived 26 volt supply is present. When the 12-volt run supply is off, Q4703 has no voltage on its base to bias it on. When the 12-volt run supply is present, Q4703 turns on and the 5-volt run supply is routed to the chassis. The 5-volt run supply also uses CR4606 as the reference voltage. Since the voltage at the cathode of CR4606 is 5.6 volts, the voltage at the anode of CR4710 is 6.2 volts. The voltage at the cathode of CR4709 is then fixed at 5.6 volts, and the voltage at the emitter of Q4703 is 5 volts.

Reg B+ is present at pin 9 of T4102, but in the standby mode, the horizontal output transistor is off. There is no load on the reg B+ supply and the voltage falls slightly to approximately 140 volts. When the set is turned on, the horizontal output transistor is turned on by the horizontal driver. The current through the high voltage transformer causes energy to be transferred to the secondary windings. One winding is used to provide both the 26 volt and the 200 volt supplies. The 26 volt supply is used as a control signal to turn on the 9-volt and 12-volt run supplies. When the 12-volt run supply is present, the 5-volt run regulator is also turned on.

On/Off Circuit Operation

The on/off operation is controlled by the system control microcomputer. The chassis is turned on by supplying Vcc to the horizontal oscillator contained in U1001. After the horizontal circuit begins operation, the scan-derived power supplies provide power to the remainder of the chassis. When the set is turned off, the Vcc to the horizontal circuit is removed.

When the set is off, Q4306 and Q4304 are off. This places a Hi at the base of the horizontal Vcc switch Q4301. When Q4301 is on, a Lo is present at the base of Q4305, keeping it off. In addition, when the set is off, Q4705 is turned on, removing the bias voltage for the 9-volt and 12-volt regulators. (The Horizontal Vcc is approximately 0.9V in the standby mode.)

When the system control microcomputer detects a power on command from either a front panel keypress or a remote command, the TV ON output port at pin 38 goes Hi. The Hi is applied to the base of buffer transistor Q4306. The Hi is coupled to the base of Q4304, causing it to turn on. When Q4304 turns on, the base resistors of Q4301 and Q4705 are essentially grounded.

Q4301 and Q4705 operate in the linear mode as error amplifiers. Q4301 and Q4705 form a feedback regulator. If the Horizontal Vcc is too high, Q4301 conducts more base current, reducing base current to Q4305. If Horizontal Vcc is too low, Q4301 conducts less, supplying more base current to Q4305, raising the output voltage.

When the scan derived 26-volt supply is present, the 9-volt and 12-volt regulator circuits begin to operate. The 9-volt supply is used to regulate the 12-volt supply. The 26-volt supply is routed through resistors to the base of both Q4702 and Q4704. CR4712 provides the reference for the 9-volt run supply. Since the emitter of Q4704 is fixed at 9 volts, the base is also fixed at 9.6 volts. By choosing the values of the resistors in the base circuit, the voltage at the base of Q4702 is also fixed at 12.6 volts. The voltage at the emitter of Q4702 is then a constant 12 volts. The 8.2 volt zener in the 9-volt regulator is used to regulate both the 9-volt and the 12-volt run supplies. Q4705 is the error amplifier for the 9 and 12 volt regulators. The operation of Q4705 is similar to the operation of Q4301.

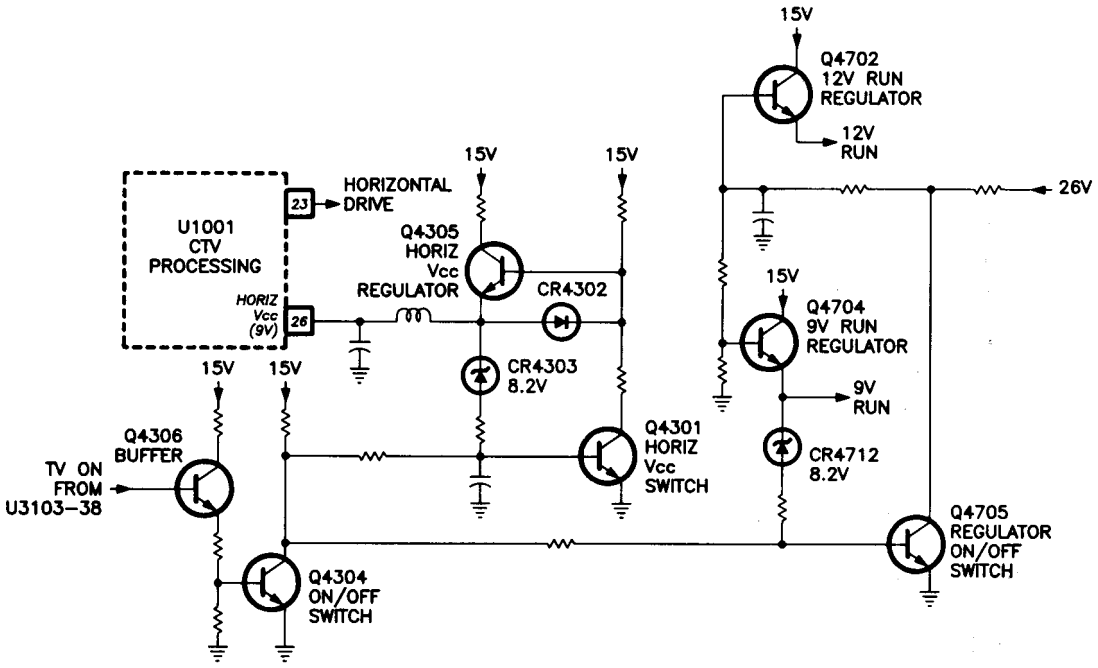


Fig. 5 On/Off Circuit

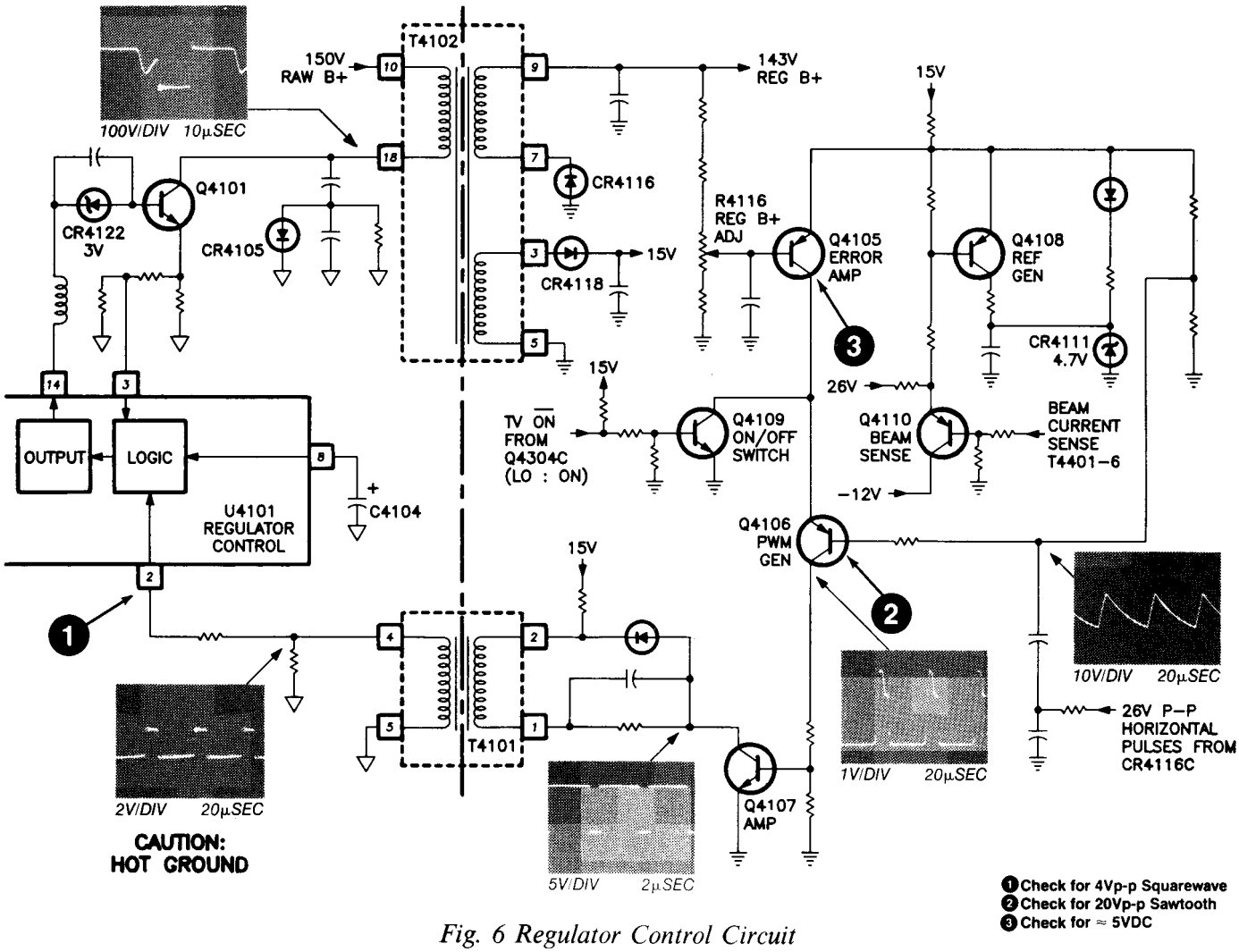


Fig. 6 Regulator Control Circuit

Regulator Control Circuit Operation

The regulator control circuit is used only when the set is on. In the standby mode, the power consumption is small and the standby regulator control is used. This circuit does not provide as good regulation, but in the standby mode, tight regulation is not needed. When the set is operating, regulation is more critical, and a different regulation system is used.

In the run mode, the control system uses both the level of the reg B+ and the horizontal retrace pulses to provide a pulse-width modulated (PWM) feedback signal to the regulator control IC U4101. The PWM signal also forces the regulator to operate at a horizontal rate. If the regulator control circuit fails to operate properly, the standby regulator system attempts to keep the output voltages correct, however the regulation is not correct. The picture size will vary with the scene content, the picture will bloom when the beam current increases.

The control system consists of a reference generator, error amplifier, and PWM generator. The reference generator provides a stable voltage reference for the error amplifier. The error amplifier compares the level of the reg B+ to the reference voltage and develops a difference signal. The PWM generator uses the difference signal to change the pulse width of the PWM control signal. The control signal is amplified and transformer coupled to the regulator control IC. The PWM signal controls the pulse width of the drive pulse to the chopper output transistor Q4101.

The reference generator consists of Q4108 and CR4111. Q4108 modifies the reference voltage to compensate for changes in beam current. The reference voltage is applied to the emitter of error amplifier Q4105. Q4108 acts as a variable resistor to change the voltage at the emitter of Q4105. The voltage at the base and emitter of Q4105 determine the collector current flowing through the transistor. The beam current sense input at the base of Q4110 is connected to the high voltage resupply input of the high voltage transformer. This input tracks the beam current. As the beam current increases, the voltage at the base of Q4110 decreases. Q4110 shifts current away from the diode branch, lowering the reference voltage.

The error amplifier compares the level of the reg B+ supply to the reference voltage. The reg B+ is passed through a resistor divider and the level is sampled and applied to the base of the error amplifier. The reference voltage is applied to the emitter of Q4105. The output of the error amplifier is a DC level which is routed to the emitter of PWM generator Q4106. The DC level represents the difference between the reference level and the reg B+ level.

The input at the base of the PWM generator is a horizontal rate ramp added to a DC level. The horizontal rate ramp is developed integrating a 26Vp-p horizontal pulse from the high voltage transformer. The DC level is derived from the reference voltage. The ramp is AC coupled to the base of Q4106. Q4106 conducts when the sum of the ramp and the DC level are 0.6V below the output of the error amp. When the Reg B+ supply drops, Q4105 conducts more and raises the error voltage. This increases the portion of the ramp that is 0.6V below the voltage at Q4106-E. Q4106 is on longer, which ultimately increases the on time of the chopper. The signal at the secondary of T4101 is applied to the logic circuit in U4101 to vary the duty cycle of the output pulses. By controlling the duty cycle of the output pulses, the level of the reg B+ supply can be tightly regulated.

The PWM output of T4101 varies the duty cycle of Q4101. The amount of time that Q4101 is on determines the amount of energy transferred to the secondary supplies. The network at the base of Q4101 ensures that the proper waveform for both the turn on and turn off of Q4101 is present. The snubber network at the collector of Q4101 slows the rise time of the kickback spike that occurs when Q4101 turns off.

The on/off switch Q4109 was added to turn the regulator off when the set is turned off. The horizontal yoke and retrace capacitor form a tuned circuit. When the horizontal circuit is turned off, the tuned circuit tends to ring at a low frequency rate while the voltage collapses. This ringing caused the regulator to operate erratically. Q4109 was added to ensure that the regulator goes back to the standby mode when the set is turned off. When the set is turned off, the signal at the base of Q4109 goes Hi, causing Q4109 to turn on. When Q4109 is on, the PWM generator is held off. When the PWM signal is removed, the regulator goes back to the standby mode.

Troubleshooting Strategy

The standby circuit must operate normally before malfunctions in the regulator control circuit can be diagnosed. See the section on B+ regulator standby circuit operation before attempting to diagnose a problem in the regulator control circuit.

If a problem in the regulator control circuit is suspected, confirm the presence of the PWM feedback signal at U4101 pin 2. If the pulses are present, the regulator control circuit is probably operating normally and the problem is in some other circuit area, most likely the horizontal deflection circuit. If the PWM signal is missing, check for the 26Vp-p horizontal rate ramp at the base of Q4106. If the ramp is missing, suspect a problem in the horizontal deflection circuit. If the pulses are present, Check the DC voltage at the emitter of Q4106. If the voltage is Lo, suspect a defective Q4109 or a malfunction in the on/off circuit. In addition, the reference voltage circuit could be defective. If the voltage is approximately 5 volts, suspect a malfunction in Q4106, Q4107, or the primary circuit of T4101.

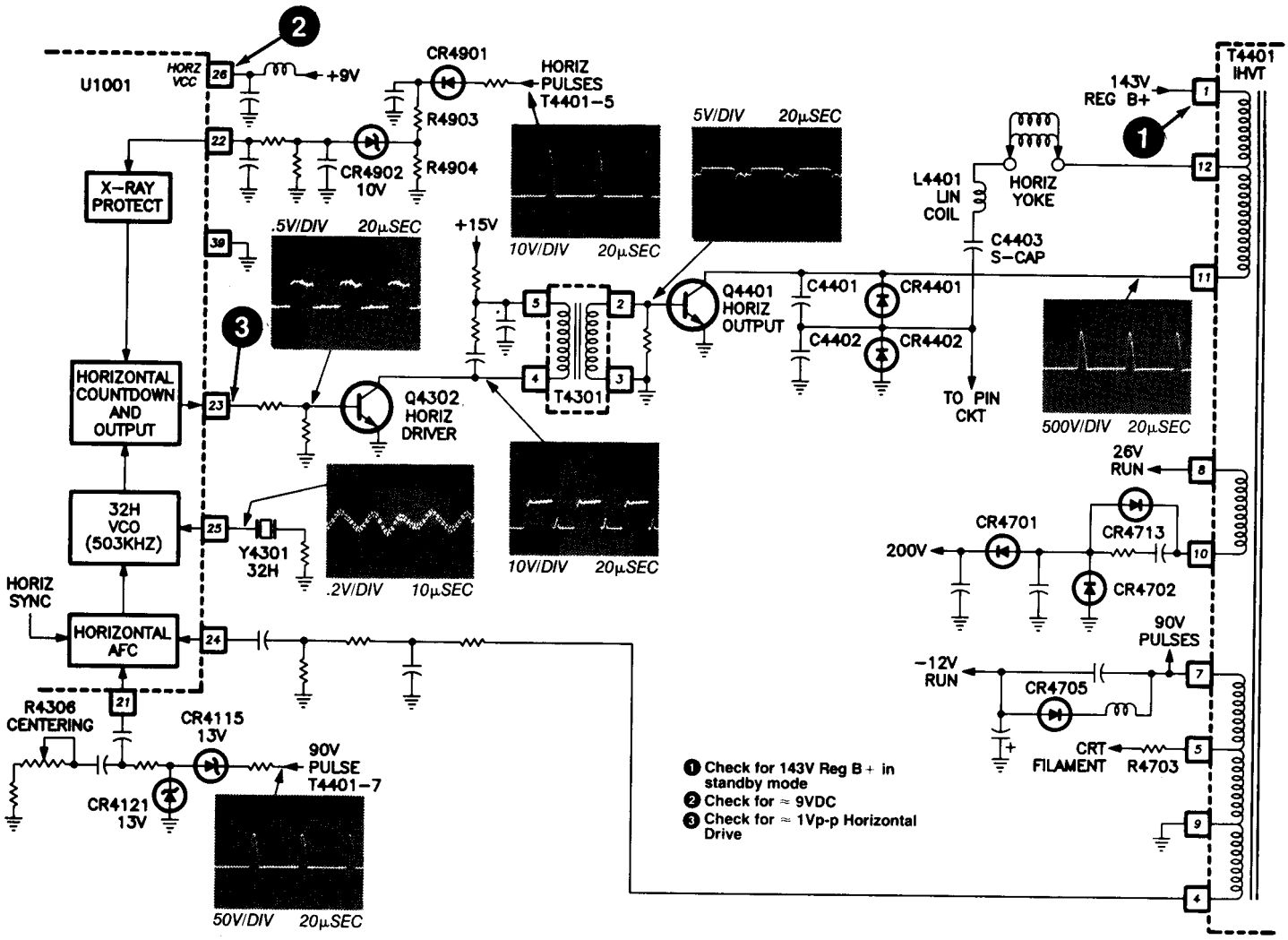


Fig. 7 Horizontal Deflection Circuit

Horizontal Deflection Circuit Operation

The circuit configuration of the horizontal deflection circuit is very similar to the design used in previous chassis. U1001 contains the horizontal countdown circuit and generates the drive signal for the horizontal driver transistor Q4302. The output of the driver is transformer coupled to the base of the horizontal output transistor Q4401. The output of Q4401 drives both the horizontal yoke and the primary of the high voltage transformer T4401.

The horizontal automatic frequency control (AFC) circuit compares the output of the horizontal circuit to the occurrence of sync. Horizontal sync is provided from the luminance processing portion of U1001. A sample of the horizontal output pulse is supplied from pin 7 of T4401 to an integrator circuit. The output of the integrator is a sawtooth waveform. The sawtooth is compared to a fixed reference voltage. The output of the AFC circuit is a control voltage applied to the 32fH voltage controlled oscillator. The AFC circuit modifies the signal from the VCO to phase lock the horizontal deflection frequency to the incoming sync signal. The horizontal phase control changes the time constant of the integrator, changing the slope of the sawtooth applied to the AFC circuit. If the slope increases, the video is shifted to the left of the raster and a decrease in the slope moves the video to the right. An additional sample of the horizontal output pulse is applied U1001-24. This pulse is used by the anti bend circuit to compensate for horizontal width changes caused by variations in the scene brightness.

The frequency of the horizontal oscillator is determined by ceramic resonator Y4301. The output of the crystal is 32 times the horizontal frequency (503kHz). The output of the VCO circuit is applied to the horizontal countdown circuit. The countdown circuit divides the 503kHz signal to the proper frequency for the horizontal deflection circuit (15,734Hz). The horizontal drive output of the countdown circuit is amplified and exits U1001 at pin 23.

The output signal from U1001 is applied to the base of the horizontal driver transistor. The signal at the collector of Q4302 is transformer coupled to the horizontal output transistor Q4401. The power for the horizontal driver stage is supplied by the switching regulator 15-volt supply. This supply is present for both the standby and run modes.

The 9-volt input at pin 26 is the power source for the horizontal deflection and X-ray protection circuits in U1001. This is a switched supply and is controlled by the on/off circuit. The receiver is turned on by supplying 9-volts to the horizontal circuit. If the horizontal circuit fails to operate, none of the run power supplies are present.

X-Ray Protection
One of the windings in the high voltage transformer is used to track the high voltage supply. The pulses at pin 5 of T4401 are rectified by CR4901, charging the capacitor. A rise in the high voltage causes a rise in the detected voltage. The detected voltage is applied to a precision voltage divider network. The voltage at the junction of R4903 and R4904 is then applied to the cathode of Zener diode CR4902.

CR4902 is a 10-volt Zener diode. To activate the X-ray protection circuit, the voltage at the cathode of CR4902 must exceed the XRP threshold voltage. The threshold voltage is about 11.5 volts, 10 volts for CR4902 and 1.5 volts to activate the circuit in U1001. During normal operation, the voltage at pin 22 is low. When the voltage at pin 22 rises above 1.5 volts, the X-ray protection circuit disables the output from the horizontal countdown stage.

When the horizontal circuit stops operating, the 26 volt run supply is no longer produced. The loss of the 26-volt supply causes the 9-volt run regulator to turn off. The system control microcomputer detects the loss of the 9-volt run supply and turns the set off. The XRP circuit in U1001 contains an SCR latch. The Horizontal Vcc must be removed in order to reset the circuit. The microcomputer removes the Horizontal Vcc and then attempts to restart the set. The microcomputer turns the set on for about 1/4 second and then off for about two seconds. If the 9-volt supply is present, the set stays on. If the 9-volt supply is missing, the on/off cycle is repeated. If the startup cycle is repeated three times within one minute, the microcomputer keeps the set off. The set will not attempt to restart until AC power is removed to reset the microcomputer.

Shutdown Troubleshooting
The program in the system control microcomputer has been changed for shutdown conditions. In the past, when the XRP input to the microcomputer changed state, the microcomputer caused the set to cycle on and off. In the CTC168/169 chassis, the microcomputer counts the number of times the fault detect input at pin 2 of the microcomputer goes Lo. If the signal at pin 2 goes Lo three times within one minute, the microcomputer keeps the set off until AC power is removed.

A shutdown symptom can also be diagnosed as a dead set symptom. In addition, the fault detect input also monitors the 10-watt per channel audio circuit for malfunctions in the audio output stage. A problem in the audio circuit can cause the same symptom as an X-ray shutdown condition. Begin troubleshooting by removing AC power to reset the system control microcomputer. Turn the set on and listen for the high voltage to come up. In most cases of X-ray shutdown, it is possible to hear the high voltage come up before the set shuts down. Refer to the audio portion of this manual for the procedure to safely disable the audio shutdown circuit. If the shutdown problem goes away, the problem must be in the audio circuit. If the shutdown condition remains, the malfunction could be caused by an open retrace capacitor, a fault in the X-ray detect circuit, or a problem in the regulator causing the reg B+ supply to rise.

The reg B+ can be checked in the standby mode. In the run mode, the reg B+ is approximately 143 volts. In the standby mode the voltage decreases slightly to about 140 volts. If the voltage is much higher or lower than 140 volts in the standby mode, correct the problem in the regulator circuit before trying to correct a malfunction in the horizontal deflection circuit.

The horizontal drive signal is coupled through the horizontal driver transformer T4301 to the base of the horizontal output transistor Q4401. The output at the collector of Q4401 is used to drive both the primary of the high voltage transformer and the horizontal yoke windings. The secondaries of the high voltage transformer develop a variety of outputs to power various portions of the chassis.

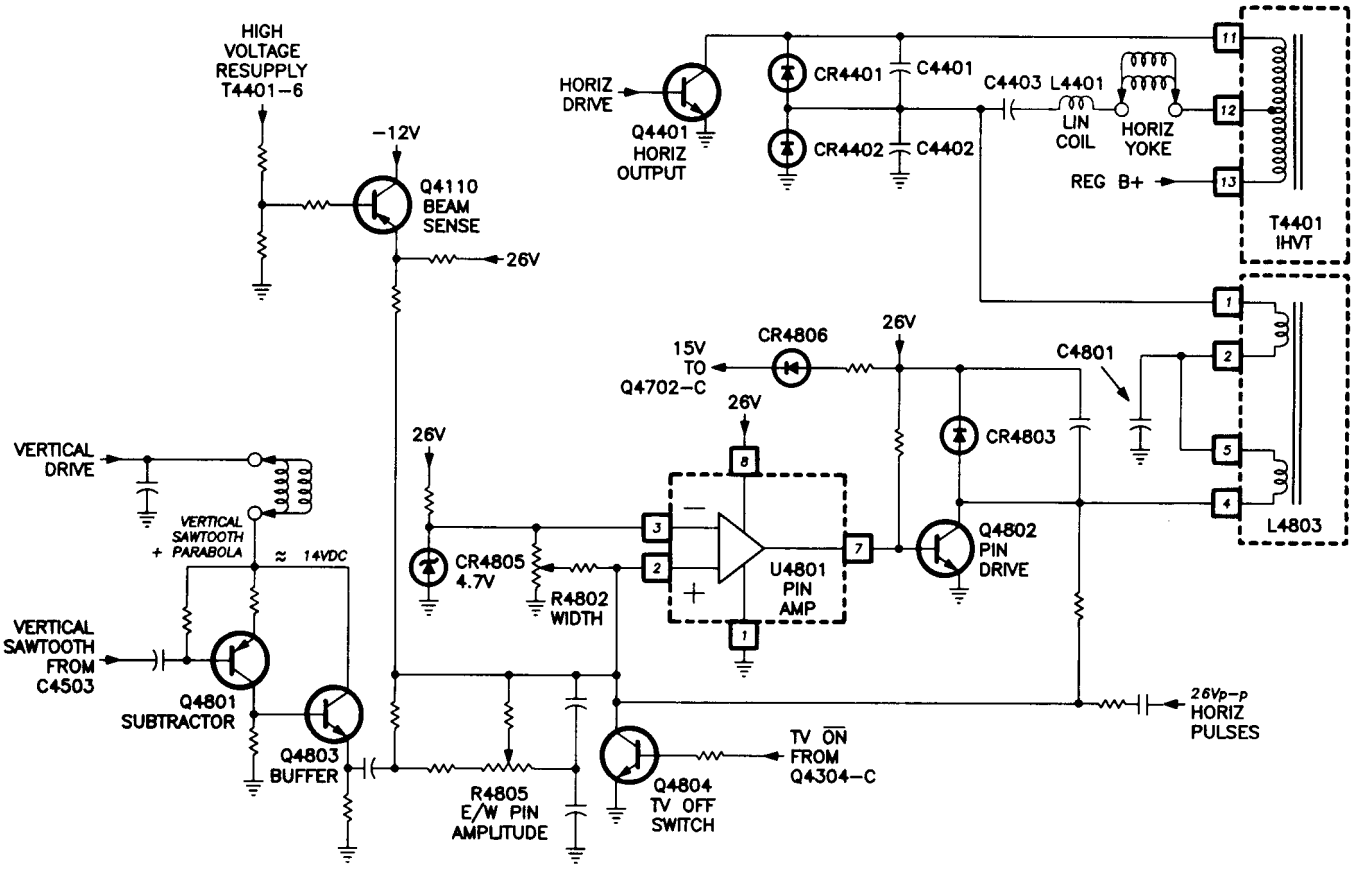


Fig. 8 Pincushion Correction Circuit

Pincushion Correction

The electron beam scanning the face of the tube must travel further in the corners than it does at the center of the screen. The pincushion correction circuit modulates the horizontal yoke current at a vertical rate to correct for the distortion caused by the physical shape of the face of the picture tube. The pincushion correction circuit is used in 27″ and larger screen sizes for direct view sets. For sets smaller than 27″, the conventional linearity coil and pin corrected yoke provide the necessary correction.

The correction circuit develops a parabola shaped waveform at C4801. By modulating the voltage on C4801, the yoke current can be modulated without affecting the high voltage. When Q4802 is conducting, the voltage across C4801 decreases. The voltage dropped across the yoke increases when the voltage on C4801 decreases. The width increases as more of the B+ appears across the yoke.

The input to the control circuit is a vertical sawtooth and a signal from the return side of the vertical yoke. The control circuit needs a vertical parabola input to make the needed corrections. The signal from the vertical yoke contains both a vertical parabola and a vertical sawtooth. This signal is applied to the emitter of Q4801. The sawtooth applied to the base of Q4801 is subtracted from the signal at the emitter. The output at the collector of Q4801 is a vertical parabola. The signal is routed through buffer Q4803 to the input of the pin amplifier U4801. East/West pin amplitude control R4805 determines how much of the vertical parabola is input to the pin amplifier. Width control R4802 sets the DC operating point of the pin amplifier. The beam current input to the pin amplifier allows the pin correction circuit to compensate for changes in width caused by variations in the beam current.

Q4802 acts in many ways like a chopper. Energy is stored in L4803. When Q4802 turns off, a reverse voltage is generated. The voltage at the collector of Q4802 rises. When the voltage reaches 26.6V, the energy is dumped into the 26V supply.

U4801 generates the PWM signal to drive Q4802. A 26Vp-p horizontal pulse is used to generate a horizontal rate ramp. The control circuit provides the vertical-rate input. The horizontal and vertical rate inputs are used to change the conduction time of Q4802 and thus vary the width.

TV Off switch Q4804 keeps the pincushion correction circuit from operating when the set is turned off. When the set is turned off, the horizontal circuit rings for a short time as the fields collapse. This ringing can affect the operation of the circuit as it switches from the run mode to the standby mode. Q4804 prevents the pin circuit from ringing and stressing Q4802. Q4804 is off when the set is running. When Q4804 turns on, pin 2 of U4801 is pulled Lo. A Lo at the input causes the output to also go Lo, keeping Q4802 off.

Troubleshooting Strategy

Most malfunctions in the pin correction circuit result in the same symptom, the raster goes to maximum width and appears to be bowed out in the center. Begin troubleshooting by varying the settings of both the width and the E/W Pin Amplitude controls and monitoring the screen. If there is no change in the picture, the malfunction is most likely to be located after the input to the pin amplifier U4801. Suspect a shorted pin output transistor Q4801. If changing the controls changes the picture but the raster cannot be set to the correct width or always appears bowed, suspect a malfunction in the vertical parabola, either Q4801, Q4803, or a leaky CR4805.

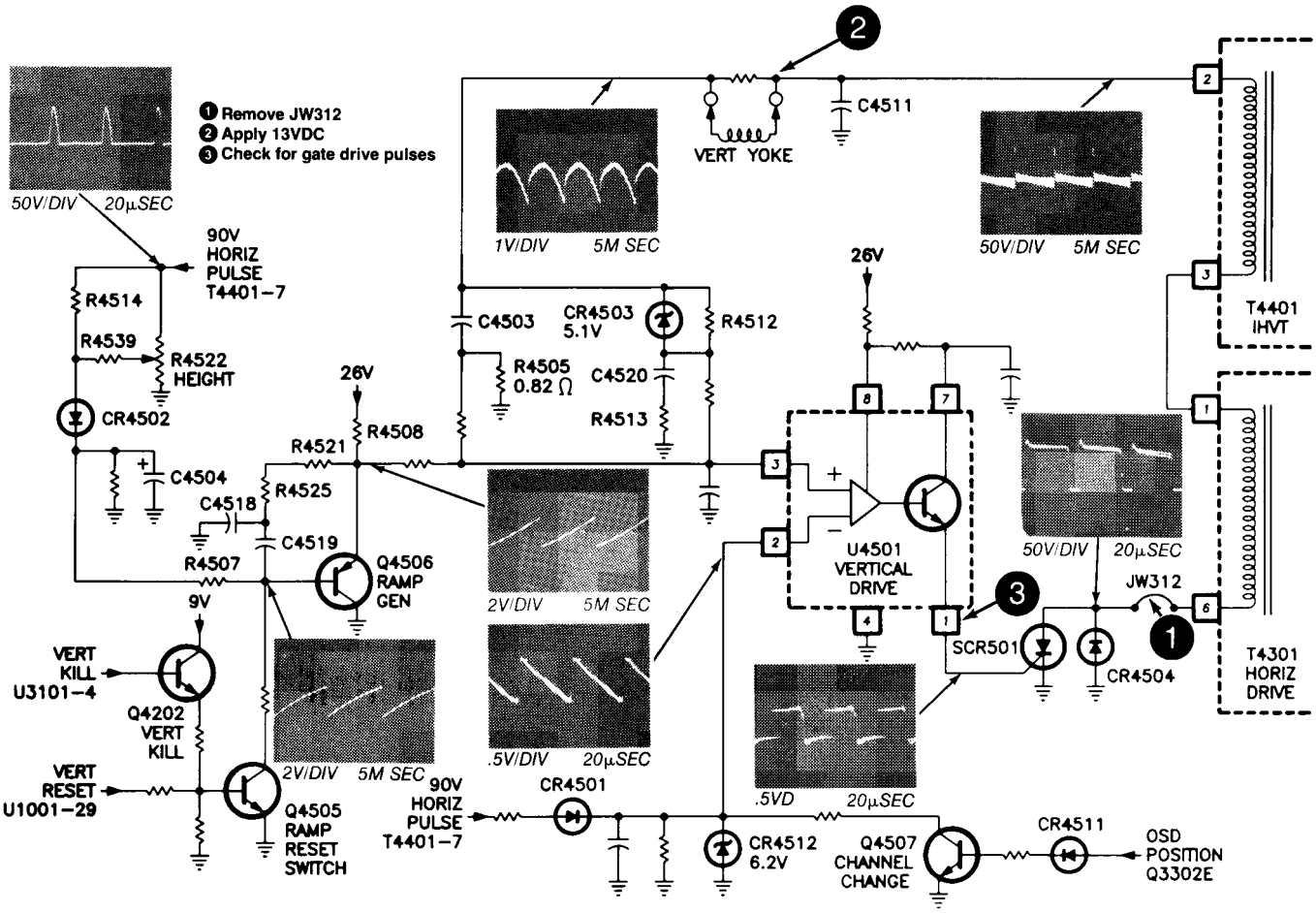


Fig. 9 Vertical Deflection Circuit

Vertical Deflection Circuit Operation

The vertical deflection circuit used in the CTC169 chassis is very different from previous designs. The vertical circuit uses a horizontal pulse from the high voltage transformer to provide the current for vertical scan. A diode and SCR determine the current supplied to the vertical yoke winding. A comparator provides the voltage to phase conversion to provide the gate drive pulse for the SCR. A horizontal rate pulse provides a reference to the comparator. The ramp generator develops the error signal input to the comparator. The error signal is compared to the reference to determine when the SCR is turned on during each horizontal line. The SCR is turned off by the horizontal retrace pulse.

Ramp Generator Operation

The vertical reset pulse is developed by the vertical countdown circuit in U1001. The pulse is approximately 10 microseconds long at 6Vp-p. This pulse turns Q4505 on, placing a Lo at the base of Q4506. When Q4506 is on, the ramp capacitors C4518 and C4519 are discharged through Q4505. When Q4505 turns off, the ramp capacitors begin to charge. The charging current is supplied by a power supply derived from the high voltage transformer. Horizontal pulses from the high voltage transformer are rectified by CR4502 and filtered by C4504 to form a DC supply. Height control R4522 sets the level of the DC supply. At minimum height, approximately 22 volts is present at the cathode of CR4502. At maximum height, the voltage increases to approximately 33 volts. When this voltage is applied, C4519 begins to charge.

As C4519 begins to charge, a increasing sawtooth waveform is present at the emitter of Q4506. C4518 also begins to charge. This capacitor provides nonlinear feedback to the ramp capacitor to modify the ramp at the emitter of Q4506. This feedback causes the ramp to bow slightly, providing the necessary correction for the vertical yoke. The ramp is applied to the non-inverting input of an operational amplifier in U4501, the vertical drive IC.

Vertical Drive Operation

The vertical drive IC U4501 provides a voltage to phase conversion. The vertical rate ramp from the ramp generator is applied to the non-inverting input. A horizontal rate ramp is applied to the inverting input at pin 2. Horizontal rate pulses from the high voltage transformer are rectified by CR4501 and charge a capacitor during horizontal retrace. CR4512 limits the maximum voltage to 6.2 volts. During horizontal trace, the voltage on the capacitor discharges. The comparator in U4501 determines when to provide a gate pulse to the SCR on each horizontal line. Transistor Q4507 is turned on by the system control microcomputer during channel change. During channel change, vertical sync is missing, and the countdown circuit goes to its default setting. The on-screen display tends to rise higher on the screen. Q4507 forces the on-screen display back to its normal position until a valid sync signal is received. Once a valid sync signal is received, U1001 resumes normal operation, and the system control microcomputer turns Q4507 off.

Vertical Scan Operation

The power for vertical trace and retrace is provided by a dedicated winding in the high voltage transformer. If the SCR is ignored, CR4504 and the winding between pins 2 and 3 of the high voltage transformer form a scan derived power supply. If there is no load on the system, the voltage on C4511 would be approximately 160 volts. The winding in the horizontal driver transformer limits the peak currents in the vertical circuit.

During horizontal retrace, pin 2 of T4401 is positive with respect to pin 3. CR4504 is forward biased, and C4501 is charged. During horizontal trace, pin 2 is negative with respect to pin 3, and CR4504 is reverse biased. By controlling the on time of SCR501, the voltage at C4501 can be varied from 160 volts if the SCR never turns on to 0 volts if the SCR conducts constantly. By modulating the turn on time of the SCR the proper voltage for vertical scan is achieved. The path for the yoke current is from pin 2 of T4401 through the yoke, through a coupling capacitor and current sense resistor R4505 to ground. The resistor network connecting the low side of the yoke to pin 3 of U4501 provides the DC feedback path.

The gate pulse to turn on the SCR is developed by the comparator in U4501. The vertical rate ramp is compared to the horizontal rate signal. The vertical rate ramp is an increasing ramp, while the horizontal rate signal is a decreasing voltage. The SCR is turned on when the vertical ramp is greater than the horizontal rate input. At the start of vertical scan, the voltage at pin 3 of U4501 is at a minimum, and the SCR is turned on only at the very end of horizontal scan. At the middle of scan, the current through the yoke is zero. The SCR is turned on at approximately the middle of scan, and the current through the SCR is equal to the current through CR4504. The two currents are in opposite directions, so the result is zero current through the yoke. At the bottom of scan, the SCR is conducting for most of the horizontal scan. The SCR and CR4504 never conduct at the same time. The SCR is turned off by horizontal retrace.

No Vertical Scan – Note: Power up without the yoke attached will result in excessive power in the resistor across the yoke, causing it to open. Always make sure the yoke is connected during troubleshooting.

Note: Any malfunction which results in no gate drive to the SCR or an open SCR causes overvoltage of C4503. There can be up to 160 volts across a part rated at 35 volts. Begin troubleshooting a malfunction of this type by removing JW312 and replacing C4503. Connect a DC power supply adjusted to about 13 volts to the high side of the yoke (E4502). Apply AC power and turn the set on. Monitor the gate drive pulses at the gate of SCR501. Gate drive pulses should be present when the supply is at 13 volts. The gate drive pulses should stop when the supply is reduced to about 10 volts, and should be continuous when the supply is adjusted above 13 volts. If these conditions can be achieved, suspect a defective SCR. If not, locate the defective components in the ramp generator or horizontal ramp circuit. When the defective components have been located and the operating conditions with the DC supply are achieved, it is safe to connect JW312.

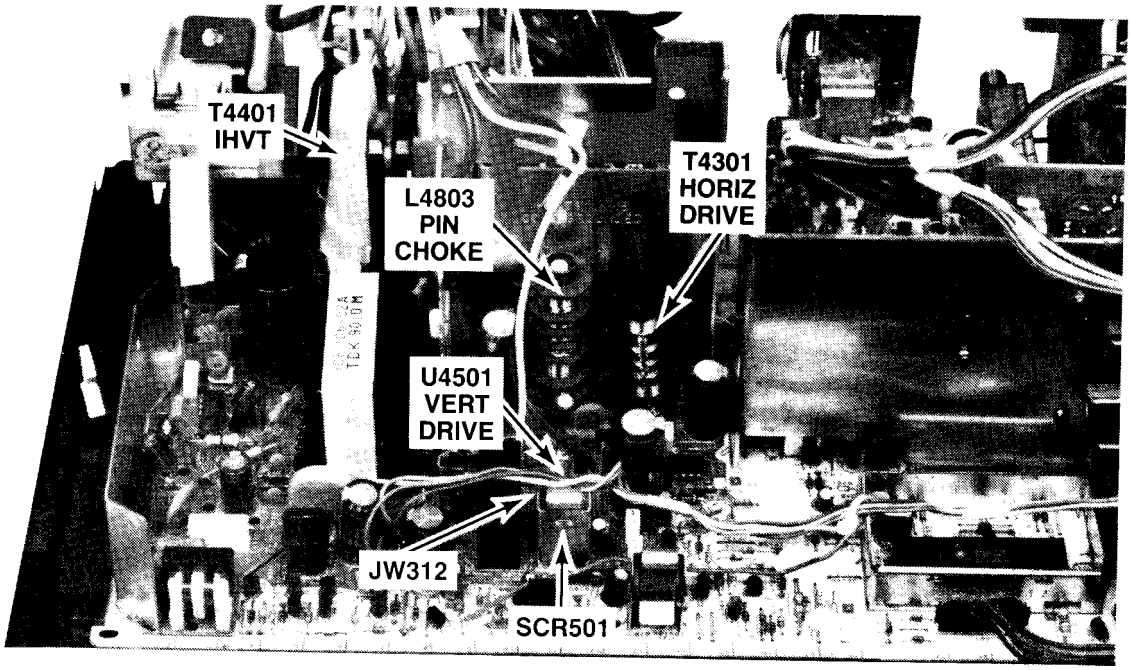
Vertical Retrace Operation

The vertical yoke and C4511 form a tuned circuit. During vertical retrace, the field in the yoke collapses and the voltage across C4511 increases. The SCR does not conduct, but CR4504 still conducts for a short time during horizontal retrace. The voltage across C4511 causes the beam to move quickly to the top of the screen and the scan cycle begins again.

Troubleshooting Strategy

Malfunctions in the vertical circuit can be group into two major categories, no vertical deflection and incorrect vertical deflection. The malfunctions covered in incorrect vertical deflection are insufficient height, poor linearity, and symmetry (vertical centering is off so the top half of scan is larger or smaller than the bottom half of scan).

- Insufficient Height – Problems in the height setting can be caused by either the power supply used to drive the ramp circuit, the ramp generator, or the horizontal rate ramp at U4501-2. Check for a change in the DC level at the cathode of CR4502 as the height control is changed from minimum to maximum. The voltage at the cathode of CR4502 should vary between 22 and 33 volts as the height control is rotated. If the voltage is missing or incorrect, suspect R4522, CR4502, or C4504. If the DC voltage is correct, check for a vertical rate ramp signal at U4501-3. If the signal is missing or incorrect suspect Q4506, C4518, and C4519. If the voltage is correct at pin 2 check for a horizontal rate ramp at pin 3 of U4501. If this signal is missing or incorrect, suspect CR4501, CR4512, or Q4507.
- Linearity – Problems in linearity are most apparent when viewing a crosshatch pattern, The blocks in the crosshatch change height from top to bottom of the screen. For problems in linearity, suspect C4503, C4520, and R4512.
- Symmetry – Problems in symmetry appear as vertical centering problems. The raster is offset so that the top half of the raster is either larger or smaller than the bottom half of the raster. Suspect R4513, R4521, and R4525.



CTC168/169 Vertical Circuit Components

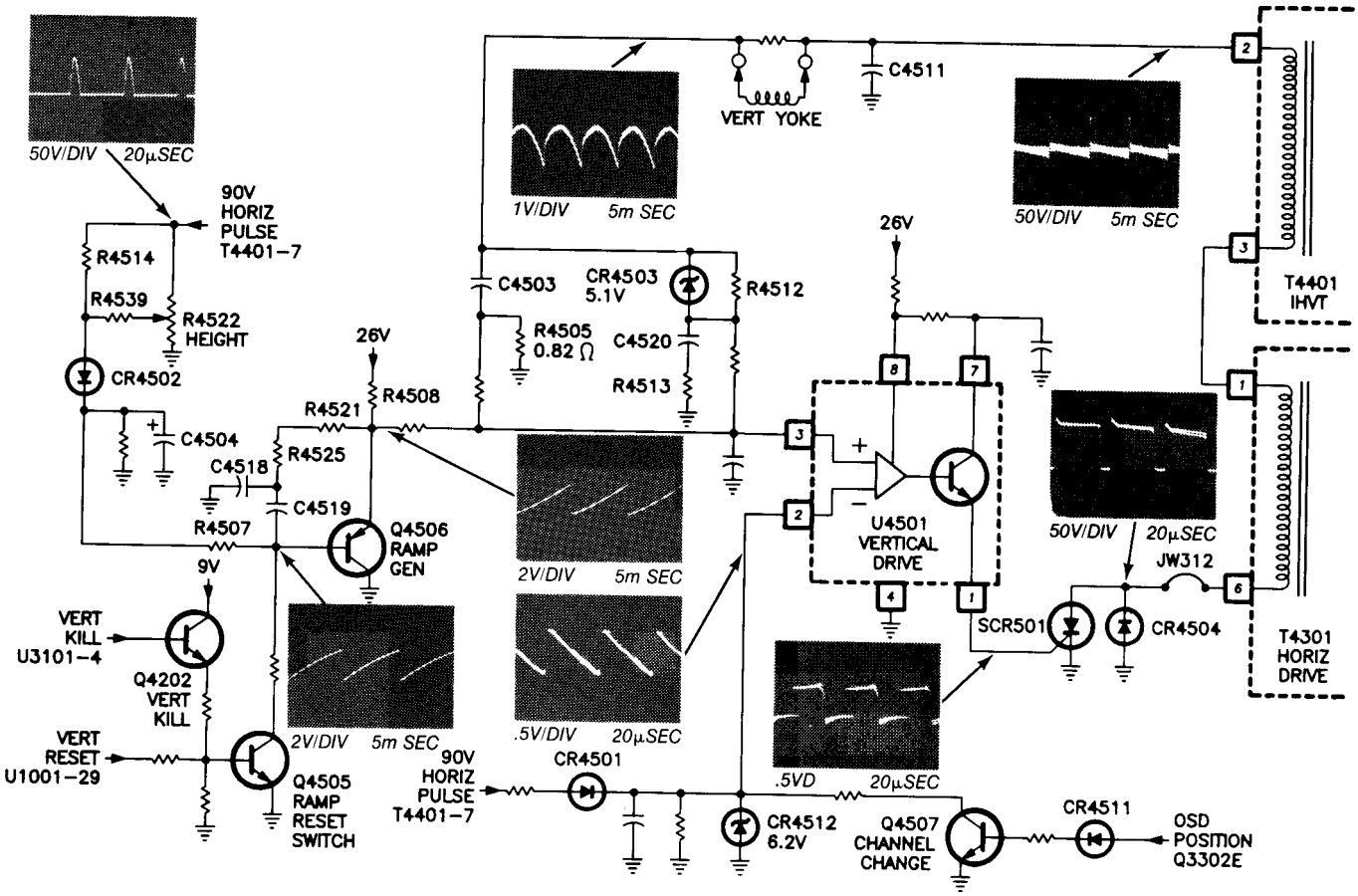


Fig. 9 Vertical Deflection Circuit (repeated)

SYSTEM CONTROL FEATURES

The following section gives a brief overview of some of the features of the CTC168/169 that are primarily system control oriented. Refer to the owners manual for a more complete explanation.

Video, Audio, and Setup Menus

Video and audio adjustments are menu driven just as in previous chassis. Pressing the video button brings the picture controls to the screen. To step through the menu, repeatedly press the video button until the desired parameter is selected. The selected parameter is highlighted with a blue background. Pressing the plus or minus keys adjusts the setting you have selected.

The menu displays 5 items on the screen at once. Once the last item on the screen is selected, pressing the video button scrolls that selection up one position and moves a new selection onto the bottom of the screen. Keep pressing the video button until no more selections appear. The same routine is used for the audio and setup menus.

Remote Static Convergence (Projection only)

Static center convergence on the CTC169 projection sets is controlled from the remote control. Press the video button until the convergence selection appears on the screen. Press the plus key to bring the small convergence crosshatch to the center of the screen. The right and left arrow symbols below the pattern indicate that the blue crosshatch may be adjusted to the right by pressing the volume up key and to the left by pressing volume down. Pressing the plus key changes the arrows to the up and down direction. Now the volume up key moves the blue crosshatch up while the volume down key moves the crosshatch down.

Pressing the plus key brings up the right/left arrows in red to allow right/left adjustment of the red crosshatch. Pressing plus again brings the red up/down arrows to the screen. Pressing plus again returns you to the blue adjustments. Pressing the minus key during this procedure takes you back to the previous adjustment if you need to back up.

Channel Labeling

The channel label feature allows you to assign a four character label to as many as 40 channels. Select the channel you wish to label. Press the setup button until you reach the channel label feature. Press the plus button and four blocks will appear below the channel number on the screen. The first block will be highlighted indicating this is the character that is being altered.

Press the volume up key to step through the alphabet. The volume down key decrements you through the alphabet. Once you reach the desired character, press the plus key to move the cursor to the next character to the right. Use the volume keys to select the character for this position. Pressing the minus key moves you to the character position to the left.

Once you have entered the characters for this channel, select the next channel you wish to label by using the channel up/down buttons or by direct entry.

The label information is stored in the EEPROM to prevent loss of the channel labels during power loss.

VCR Channel

This feature automatically selects a preprogrammed TV channel or video input whenever the remote VCR button is pressed. Suppose you have your VCR connected to Video Input 1 on the back of the set. This feature automatically selects input 1 when you press the remote VCR button.

Select the channel you have the VCR connected to, in this case TV 91. Press the setup button until the VCR Channel option is selected. The display will either display "VCR Channel : Off" or display a channel number instead of the word "Off". Press the plus button to enter the current channel, TV91, into the menu. From this point on, the TV will select TV channel 91 whenever the remote VCR button is pressed. To turn this feature off, press the minus button with the VCR Channel menu option selected.

Commercial Skip

This feature allows you to change channels during commercials (or any time) and automatically return to the channel you were watching when the commercial began.

Suppose you are watching channel 13 on the TV and a 30 second commercial comes on. You want to change channels during the commercial but you want to return to the show you were watching when the commercial began.

Press the CS button (commercial skip) button on the remote and a 30 second counter display appears at the lower right corner of the set. During the 30 seconds, you may change to any channel you desire. When the counter reaches zero, the TV automatically goes back to the channel you were viewing when you pressed the CS button, in this case channel 13. Repeatedly pressing the CS button increments the time counter by 30 seconds to accommodate variable length commercials.

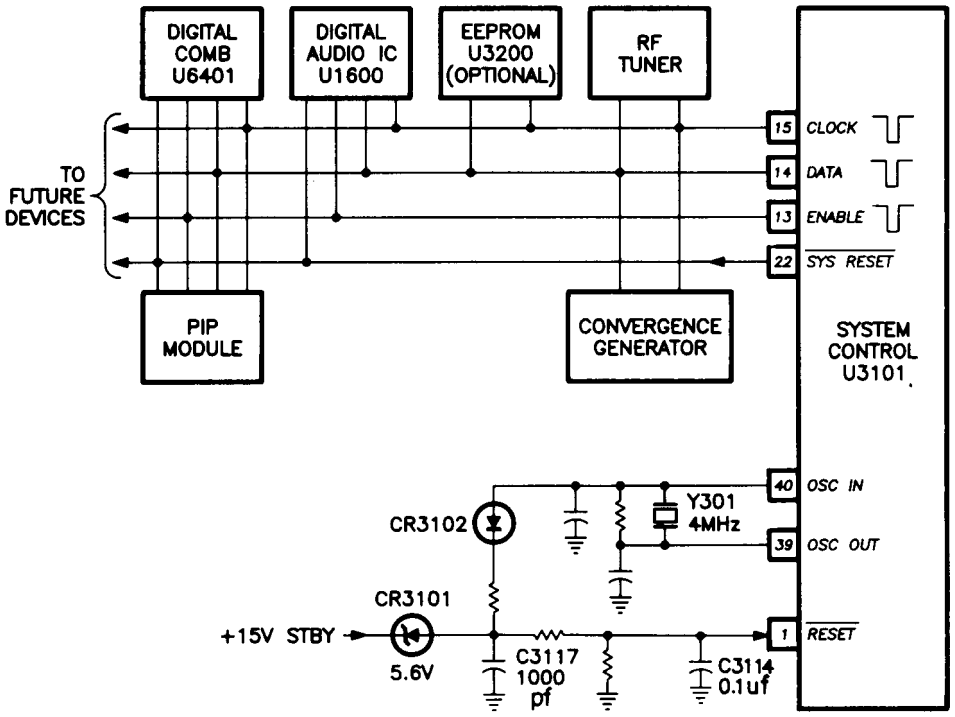


Fig. 10 System Control Serial Bus and Reset

SYSTEM CONTROL

Communications Bus

Many of the major stages of the CTC168/169 receive their operationg commands through a three wire serial communications bus from the system control micro U3101. Figure 10 shows the devices which are connected to the bus. Although the devices are tied to the same bus, there are three bus formats (IM, IIC, and ATE) implemented at different times over the bus. Note that not all devices use all three lines of the bus. The enable line is used only in the IM bus format.

The different bus formats are not distinguishable to the servicer and are beyond the scope of this manual. A brief description of the individual bus lines and the activity expected on them can be useful to the servicer.

Clock

Synchronizes the transfer of data between devices. Information on the Data line is read or transferred at the appropriate edge or level (depending upon bus format) of the clock pulse. The clock line is not a continuous signal but is only active during data transmissions. With no buttons pressed and the set on, the clock line should pulse low about 4 times every second to request stereo/SAP presence information from the digital audio IC U1600. The activity should vary when a local or remote function is executed. Similar activity can be seen on the data and enable lines.

Data

This line contains the command or status information sent between the various devices on the bus while the rest of the signals are used for timing and directing the data transfer. The viewable activity on this line is the very similar to the activity seen on the clock line as described above.

Enable (IM Bus)

The IM bus uses this line to distinguish between address and data communications on the bus. With multiple devices on the bus, individual addresses are assigned to each device. Before commands can be sent to a specific bus device, the system control micro sends the address of the desired device to inform it that it is going to be receiving a command. A low on the enable line signifies that device address information is being transmitted on the data line while a high signifies command data. The viewable activity is about the same as the clock and data lines.

Bus Troubleshooting Tip

The system control micro requests stereo presence status from the digital audio IC U1600 about four times per second over the serial bus. Check for this activity on the bus when the set is on and no buttons are pressed. The

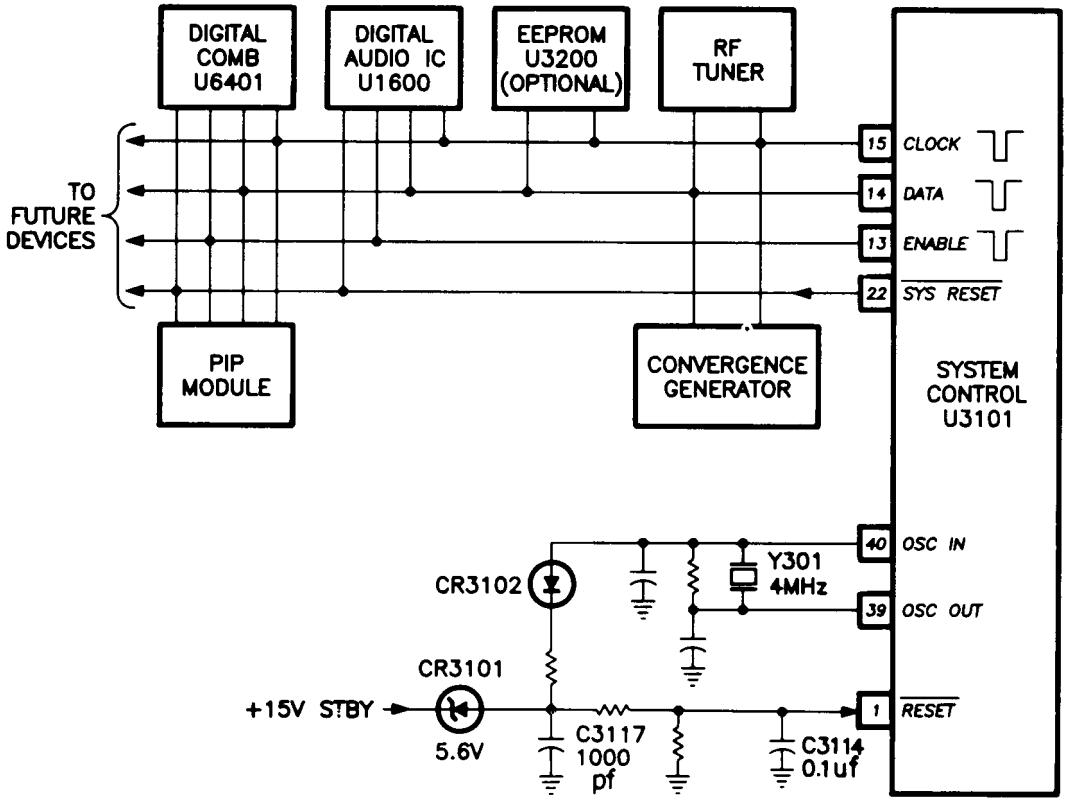


Fig. 10 System Control Serial Bus and Reset (repeated)

best way to verify proper communications bus activity is to check for 0 to 5 volt p-p signals on the clock, data, and enable lines. Intermediate voltages (between 1 to 4 volts) signify a defect on the bus.

System Reset
This line is used to reset all peripheral devices when the set is first turned on. Don't confuse this reset with the reset input at pin 1 of U3101. The system reset line is low when the set is off. When the set is first turned on, the system reset line stays low for about 1 second and goes high until the set is turned off. The peripheral devices are ready to receive bus communications after the system reset line goes high.

EEPROM

All projection sets and direct view sets with the channel labeling feature contain a EEPROM (Electrically Erasable Programmable Read Only Memory) U3200. The EEPROM is a nonvolatile memory device which means it retains its stored information even when power is lost. It can also be altered to store new information unlike ROMs (Read Only Memory) whose data is permanent.

The EEPROM stores the following information:

Channel Scan List
Sets with EEPROMs installed will be programmed with channels 02 through 13 and CH 91 at the factory. The set will *not* automatically enter autoprogram mode when turned on after an extended power loss. Autoprogramming must be initiated by the setup menu.

Sets without the EEPROM will automatically enter autoprogramming mode when turned on after an extended loss of AC Power (coldstart). The autoprogram sequence can also be initiated from the setup menu.

Alphanumeric Channel Labels
The four character alphanumeric label assigned to a channel by the customer is also stored in EEPROM. This feature is implemented only in sets with the EEPROM to prevent loss of this data.

Customer Convergence Settings (Projection only)
Projection sets allow the customer to adjust center convergence from the remote using the setup menu. The EEPROM stores a numeric value assigned to the convergence setting for the blue and red guns.

VCR Channel Setting
The VCR Channel feature automatically selects a preprogrammed channel on the TV whenever the remove VCR button is pressed. If your VCR is connected to Input 1 on the back of the set, the customer programs channel 91 into the setup menu. The TV will automatically select TV CH 91 when the remote VCR button is pressed. The channel selected is stored in the EEPROM.

RF Switch Option and Menu Format
The EEPROM is programmed in the factory to tell the system control micro whether an RF switch is installed in the set. If the RF switch is not installed, the system control micro will delete the antenna selection feature from the setup menu.

Other feature variations such as Pix-in-Pix are also stored in EEPROM as opposed to configuration code pins connected to the system control micro.

Reset

The system control micro U3101 is reset at pin 1 upon AC power application. When AC power is first applied, the 15 volt standby supply begins to rise. Before the 15 volt supply reaches its full voltage, the 5 volt standby (which is derived from the 15 volt standby supply) become active to power U3101. However, the 15 volt supply has not reached a high enough voltage to turn on CR3101. This keeps U3101 in reset since no voltage is present yet at pin 1. When the 15 Volt supply nears its full potential, CR3101 conducts to apply about 4.5 VDC to the reset pin 1.

The hysteresis within the micro (1.5 - 2.5 Volt lower to upper threshold) provides the time delay for the low to high reset transition. C3114 adds an additional delay to the rise time of the reset input. C3117 is not a significant factor in the rise time of the reset circuit.

Oscillator and Power Loss Memory Retention
The 4 MHz oscillator at pins 40 and 39 is stopped by the reset circuit during power loss to prevent discharging of the 5 volt standby supply. The longer the 5 volt supply is maintained, the longer the stored memory information within U3101 can be retained. Memory retention is guaranteed for at least 10 seconds of power loss. It will probably last a few minutes.

When AC power is lost, the oscillator input at pin 40 is pulled low through CR3102 by the resistance of the inactive reset circuit. This stops the oscillator from running. Once the reset line goes high, CR3102 is reversed biased, allowing the oscillator to operate.

System Control Functions

Since most of the system control functions are described in more detail throughout this manual, the following sections is more of a quick reference than a lengthy explanation. Figure 12 shows an overview of the pins and functions of the system control micro U3101.

Front Panel Assembly (FPA)

There are two physical sizes of front panel assemblies (FPA) used in the CTC168/169, but electrically they are identical.

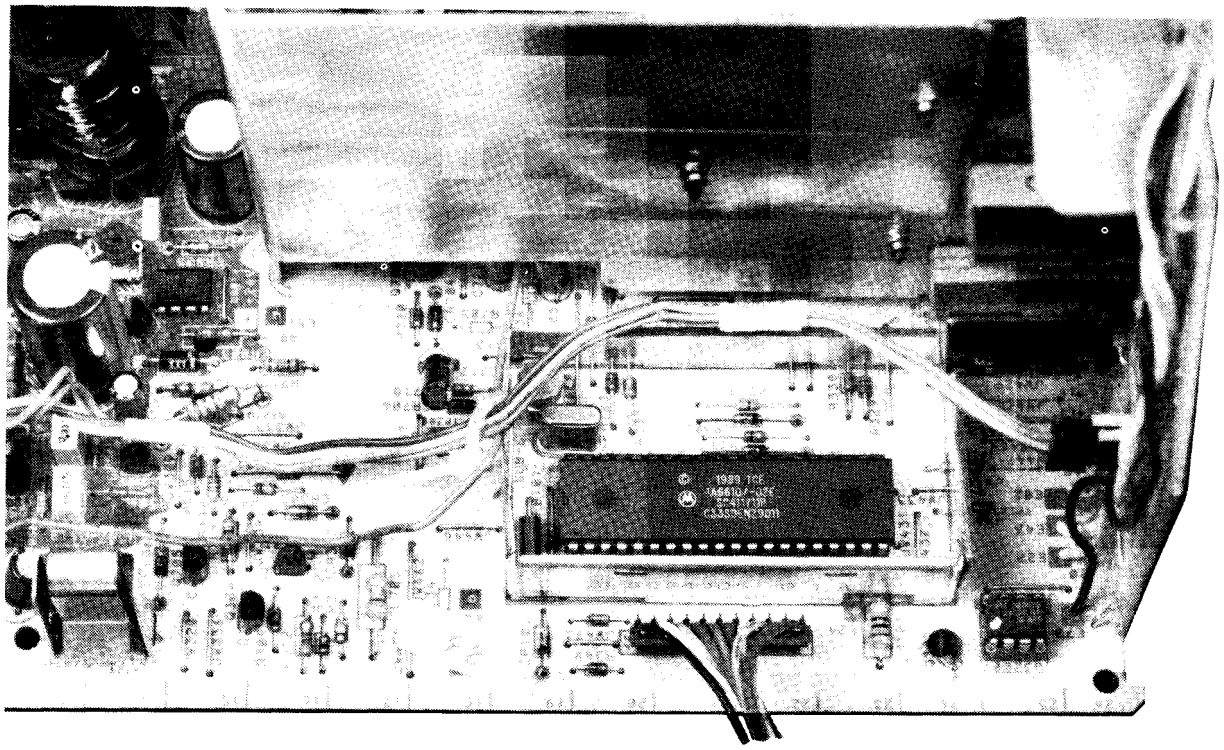


Fig. 11 System Control

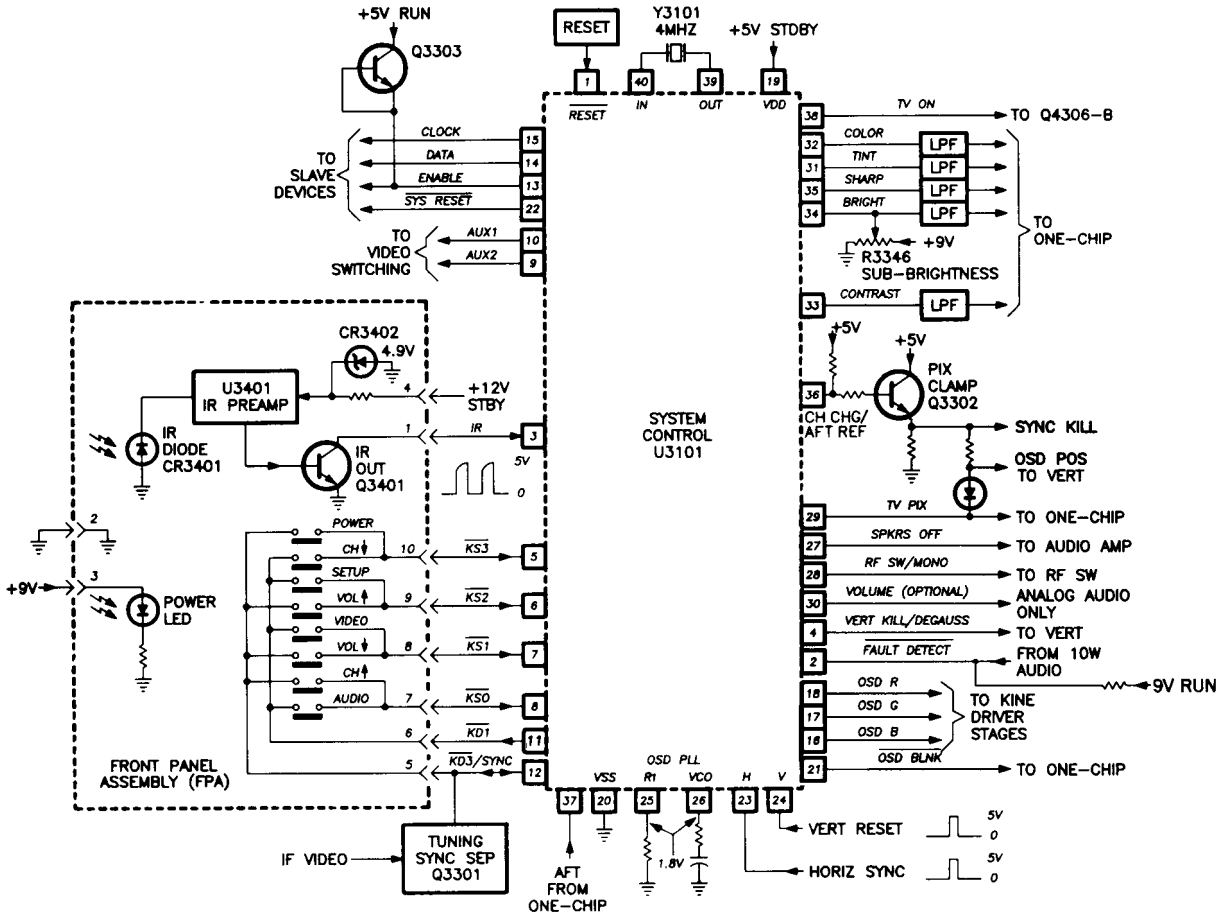


Fig. 12 System Control Functions

Keyboard Decoding

With no keys pressed, the KS0 through KS3 lines are pulled high by resistors on the main chassis. KD1 and KD3 are set low while no key is pressed. When a key is closed (pressed), a low from either the KD1 or KD3 is applied to one of the KS lines. When a low is detected at one of the KS lines, KD1 and KD3 are toggled in sequence to decode which key has been pressed.

If the power, volume up or down, and the channel button is held, KD1 will keep scanning but KD3 will remain low after the key is decoded. If Channel Down, Setup, Video, and Audio keys are held, both KD1 and KD3 continue to scan after the key is decoded.

Note: The service line for direct view picture tube bias and drive setup is displayed by simultaneously pressing both the Setup and Video keys on the keyboard with the set already on. This key press sequence displays the crosshatch pattern in projection sets. Pressing the setup button changes the color of the crosshatch.

Tuning Sync and AFT

The KD3 line is shared by the tuning sync input. When the set is on, tuned to an active tuner channel, and and no key is pressed, positive going horizontal pulses enter the micro at pin 12. These pulses are used during tuning to detect active channels. When pressing the channel up or down keys, the system control micro interrupts the keys scan sequence for about 10 milliseconds to check for sync pulses at pin 12.

The AFT input at pin 37 is used to detect AFT crossover during the tuning algorithm. Crossover is represented by 2.5 VDC at pin 37. An internal analog to digital converter within U3101 converts the analog AFT input to a digital format. The reference for the A/D converter is derived from the Channel Change/AFT Reference pin 36. During channel change, the DC voltage (5VDC) at pin 36 is read by U3101 to be used as a reference voltage for the AFT A/D converter. After pin 36 is read, it becomes an output and goes high to begin the sync kill operation during channel change.

Tuning sync and AFT are discussed in more detail in the tuning section of this manual.

IR Receiver

The FPA also houses the infra red remote receiver. CR3401 receives the IR signal which is amplified and demodulated by U3401. The demodulated IR output is buffered and inverted by Q3401 to produce the 5 Vp-p square wave for the system control micro pin 3. The system control micro decodes the signal and executes the command.

Power LED
The power on LED indicator is powered from the 9 volt run supply and not a control line from the system control micro. When the set turns off, the 9 volt supply discharges, leaving no power for the LED.

AUX1/AUX2 Controls

These lines control the switch positions of the video selection IC1401. These line do not select the audio source that goes with the video.

Communications Bus

Although this was covered in the previous sections, Q3303 bears mentioning. This transistor (diode) was added to hold the enable line low until the 5 volt run supply is established. This is needed for sets with SPIP installed. A future software change may remove the necessity for Q3303.

TV ON Control

This line goes high (5 Volts) when the set is told to turn on. The line goes low when the set is turned off. The TV ON control is tied to the base of Q4306 in the power supply section of the chassis.

Picture Control

Pins 31 through 35 of U3101 are pulse width modulated (PWM) outputs whose waveforms are filtered to produce a variable DC control voltage for the color, tint, sharpness, brightness, and contrast controls. Note that the brightness control can be preset at the factory by the Sub-brightness control R3346 to compensate for chassis tolerances during production.

Channel Change/AFT REF (Sync Kill)

The reference for the internal AFT A/D converter within U3101 is derived from is derived from the Channel Change/AFT Reference pin 36. 36. During channel change, the DC voltage (5VDC) at pin 36 is read by U3101 to be used as a reference voltage for the AFT A/D converter. After pin 36 is read, it becomes an output and goes high to begin the sync kill operation during channel change. AFT is discussed in more detail in the tuning section of this manual.

After the AFT reference is read, pin 36 of U3101 goes high during channel change to drive the sync kill line high. This turns on Pix Clamp Q3302 to apply 5 VDC to the sync kill line. The sync kill line is applied to the luma input of the one chip to bias it off, preventing noisy video from entering the sync separator during channel change and autoprogramming. This allows the horizontal oscillator in the one-chip to free run to produce a steady OSD.

TV PIX and OSD Position

TV PIX
This line goes high whenever the TV tuner is the selected video source and goes low when an external video input is selected. This line is tied to the chroma input of the one-chip to shift its DC offset to perform internal switching within the one-chip. In non PIP sets, the TV PIX line is also used as an IF defeat control when an external video is selected. In PIP sets, the TV PIX line is not used to defeat the IF since the IF must be enabled to allow the tuner to be inserted in the small pix.

OSD Position
The OSD Position control line is derived from a combination of Sync Kill and the TV PIX line. Its function is to keep the OSD from going off the top of the screen when changing channels on the TV tuner.

When the TV Pix line is high (TV selected), the sync kill line goes high during channel change. The high on the sync kill line is transferred to the vertical stage since the diode between OSD position and TV Pix is reverse biased. The high produced on the OSD position line during channel change is applied to the vertical stage. This reduces the drive to the vertical yoke which reduces the vertical size of the picture, keeping the OSD from rising to the top of the screen.

When the TV PIX line is low, (external video selected), the OSD position line is held low by the diode connected to TV PIX line. This prevents the sync kill line from affecting the OSD position during channel change from one external input to the next.

TV Speakers Off

This line goes high to turn the speakers off by removing the bias voltage to the audio power amps. When you turn the set on, the system control keeps the speakers off until about three seconds after the set is turned on. This prevents pops in the speakers as the audio circuits power up. When you turn the set off, the speakers are tuned off before the set is shut down to prevent pops as the audio circuits turn off.

RF Switch/Mono

This control line selects between antenna A or B if the set is equipped with an RF switch. A low at pin 28 selects Ant A and a high (5V) selects Ant B. Notice that this line is also labeled "Mono". The mono function may be used in future sets using an analog audio system instead of the digital audio IC.

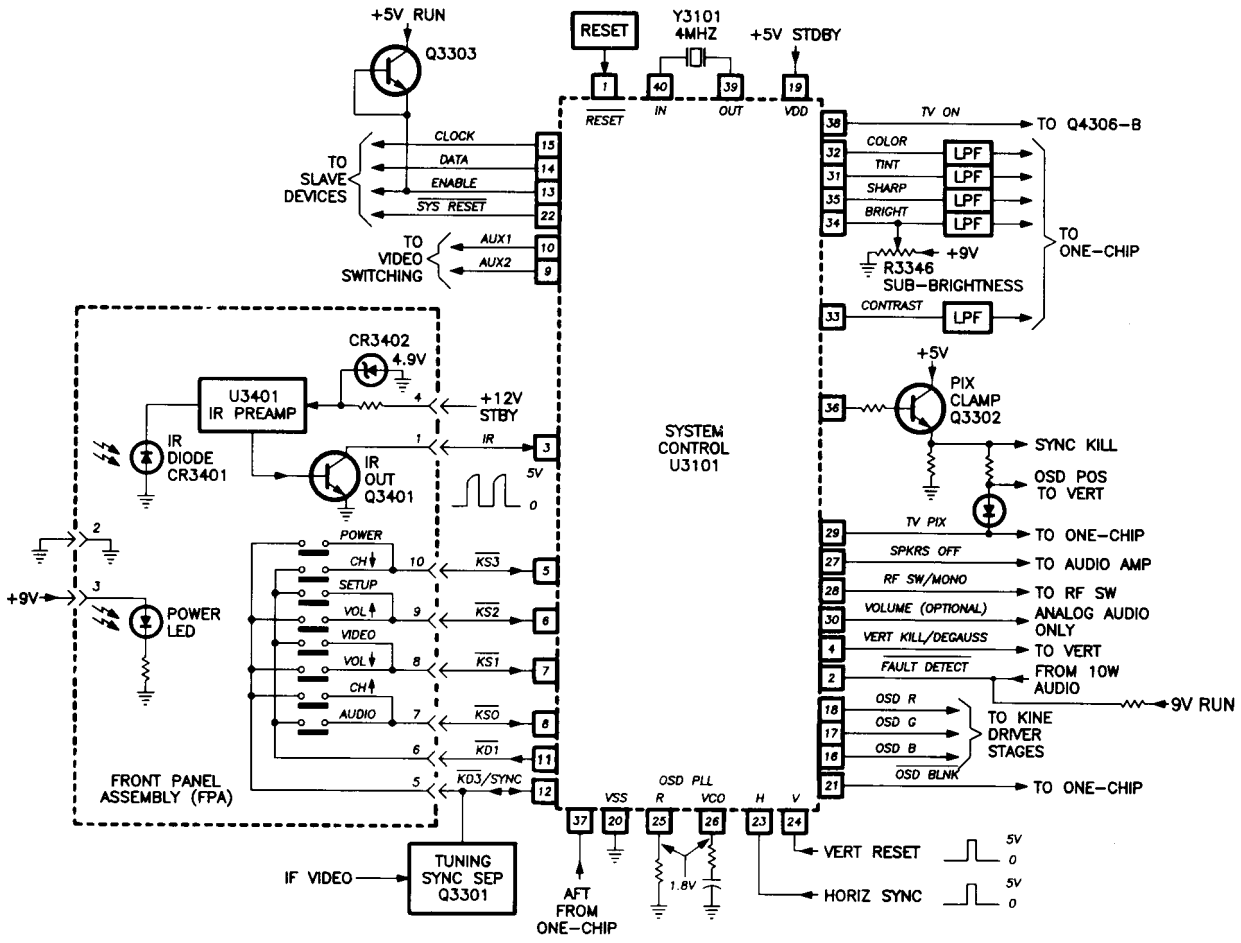


Fig. 12 System Control Functions (repeated)

Volume

Just as the mono function mentioned above, the volume pin is reserved for future analog audio sets. Currently it is not used.

Vertical Kill/Degauss

When the set is first turned on, this line goes high for about 2.2 seconds to activate the degaussing circuits in addition to killing vertical deflection. This line is high throughout the service line setup in direct view models.

Fault Detect

Whenever the fault detect input at pin 2 is pulled low, the system control micro U3101 turns the set off by pulling the TV ON line at pin 38 low. After two seconds, the system control micro turns the set back on and checks to see if the fault detect input at pin 2 has gone high. If pin 2 is still low, the system control turns the set off again. This cycle continues until the fault detect line at pin 2 goes high. The fault detect input monitors two circuits to determine whent to turn the set off.

9 Volt Run Detect

If the 9 Volt run supply from the secondary of the IHVT ever disappears due to a loss of deflection, the fault detect input at pin 2 will be pulled low by the supply. This will begin the shutdown cycle as described in the previous paragraph. The disappearance of the 9 Volt run supply could be caused by a loss of horizontal deflection due form either a defect or an X-Ray shutdown of the one-chip.

10 Watt Audio Defect Detector

Whenever a DC offset occurs in the 10 watt audio output, a fault detect circuit pulls pin 2 of U3101 low to turn the set off as described above. Refer to the 10 watt audio section of this manual for a detailed description of the Defect Detector.

On-Screen Display (OSD)

RGB Outputs and Blanking

To produce a character on the screen, one or more of the outputs at pins 16 through 18 goes high at the appropriate time. The OSD is capable of producing multiple color characters on the same line.

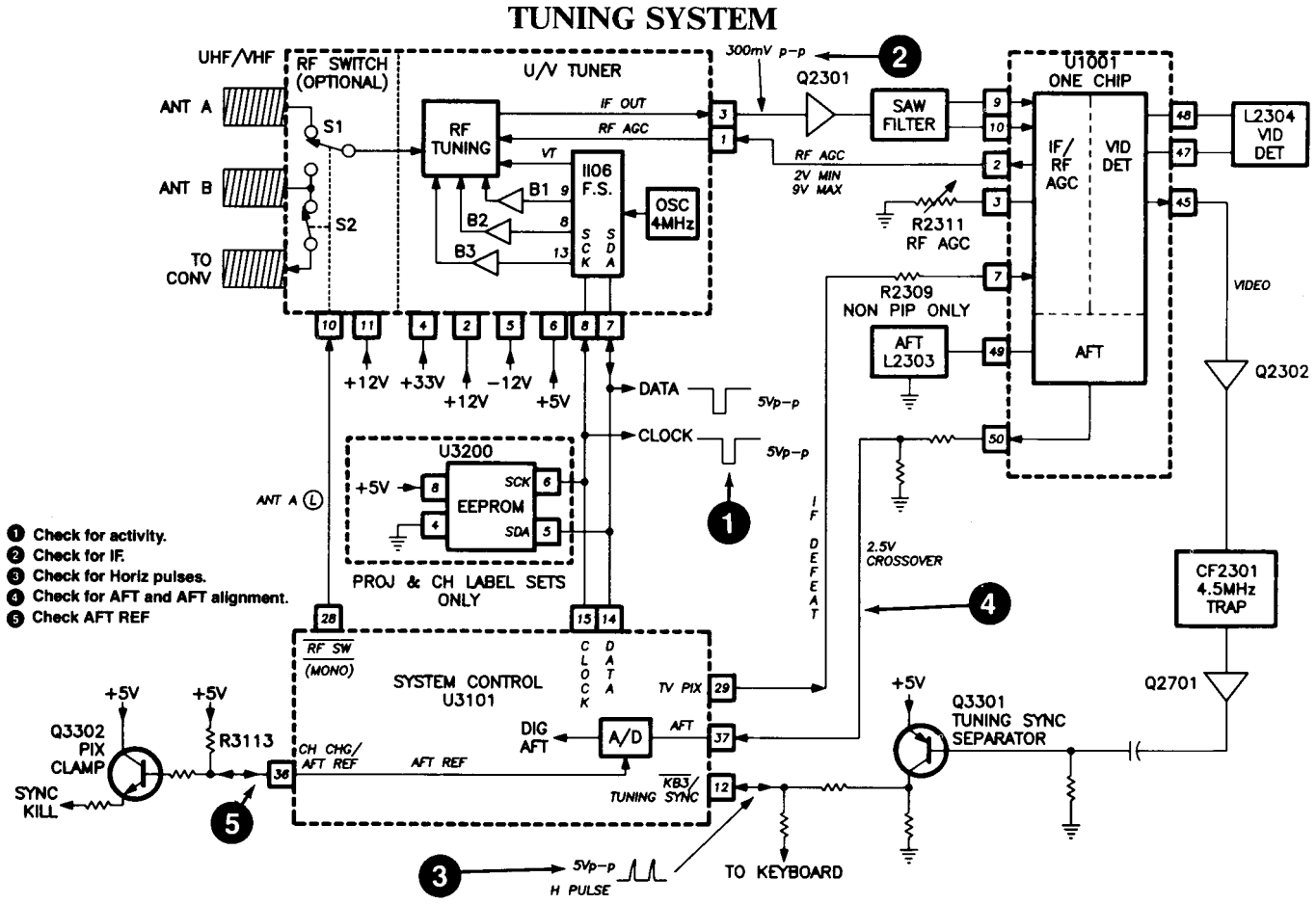


Fig. 13 Tuning Control

The OSD blanking line goes low to produce the black border surrounding the characters. This is covered in the luma processing section of this manual.

H and V Timing Inputs

The horizontal and vertical timing signals for the OSD character generation enters U3101 at pins 23 and 24. These signals inform the system control where the beam is currently scanning so it can insert characters onto the screen at the appropriate position.

If the horizontal pulse is missing, no characters will be produced. If the vertical pulse is missing, the characters will roll vertically.

VCO and R1

These pins are external control pins for the horizontal PLL within U3101. The voltage at these pins are typically around 1.8 VDC. If the voltage at the VCO pin 26 is too low, characters, will disappear. If the voltage at R1 is too low, the characters will tear horizontally on the screen.

System Control Troubleshooting

There are a few quick checks to make to verify basic operation of system control.

1. Check for oscillator at pins 39 and 40.
2. Check for a high on the reset pin 1.

If either of these checks failed, nothing else in system control can operate. If both check passed, you must check for operation of the control lines going to and from the micro as described in this and other sections of this manual.

Tuning Control Overview

Figure 13 shows the tuning control loop for the CTC168/169 chassis. Notice that unlike the tuning system in the CTC157-159 series, all band switching and tuning voltage generation is done within the tuner. The tuning commands are received through the clock and data lines from the system control micro U3101. The output of the tuner is the IF frequency of 45.75 MHz. This is very similar to the tuning system of the TX81 chassis which is currently being used in some 9" and 13" RCA and GE sets.

RF Switch (Optional)

Two tuner options are available in the CTC168/169 chassis. The MTP-M-2016 tuner is a cable ready tuner with one single input for UHF/VHF and cable. The MTP-M-2030 is identical to the 2016 except for an optional RF switch mounted on the front of the tuner. There are two RF inputs, ANT A and ANT B, and one cable converter output.

To utilize the cable converter output, connect the main cable signal to Ant B input. Select Ant A from the on-screen menu of the TV. Selecting Ant A closes S2 to sup-

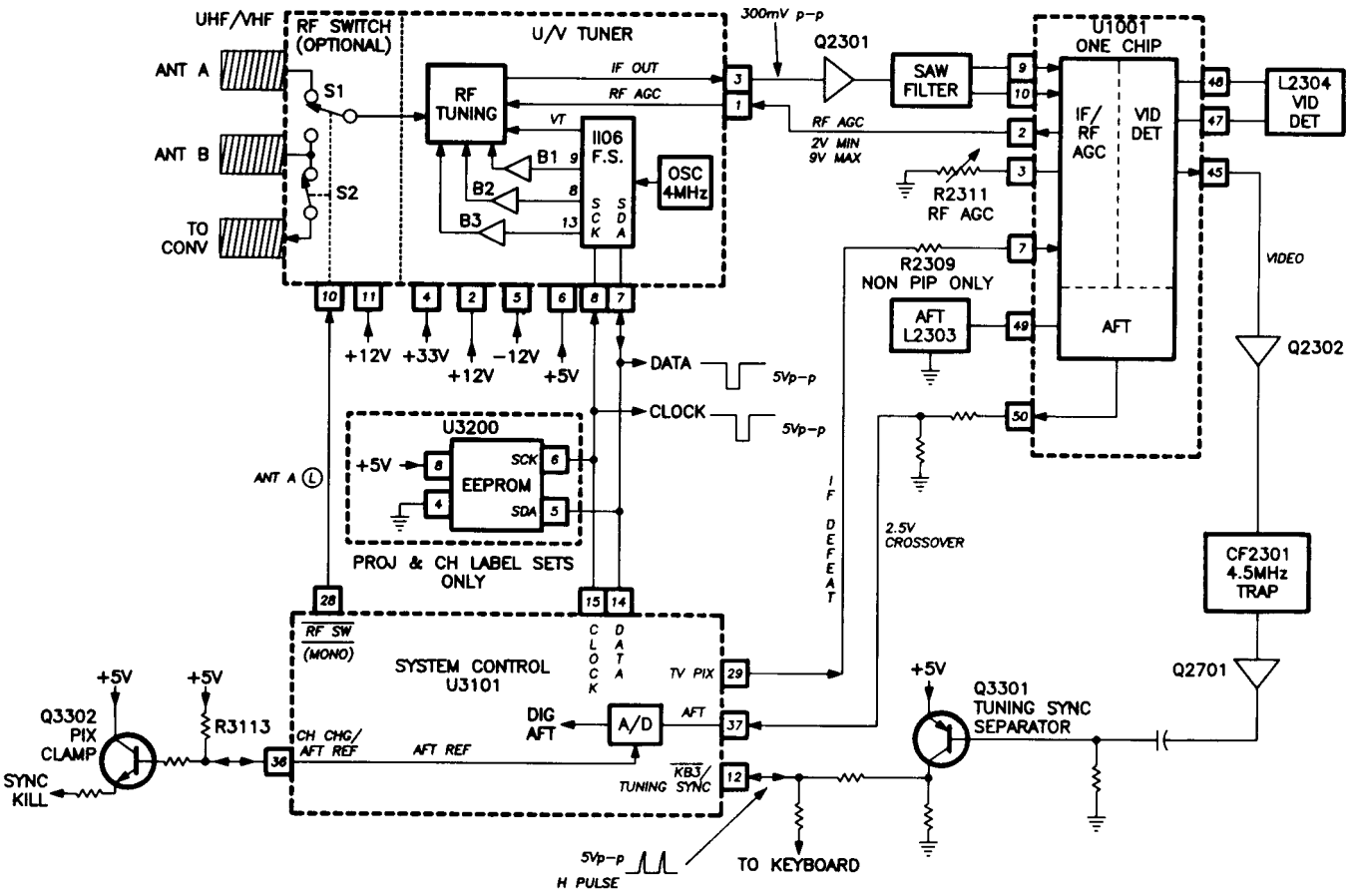


Fig. 13 Tuning Control (repeated)

ply the signal at the Ant B input to the cable converter connector. The converter output is applied to the input of the cable converter box. The output of the converter box is connected to the Ant A input which passes the signal through S1 to the tuner input.

When Ant B is selected, S2 opens to break the converter loop and S1 applies the signal at the Ant B input directly to the tuner input.

The control line at pin 10 of the RF switch module selects the positions of S1 and S2. A low at pin 10 selects Ant A and a high (9V) selects Ant B. Notice that this line is called RF SW (Mono) on the system control micro pin 28. The mono function may be used in the future for sets using an analog audio system instead of the digital audio IC currently in use for the CTC168/169. At the time of this printing, the mono option for pin 28 is not used.

U/V Tuner

The RF tuning portion of the tuner receives its input either directly for the antenna connection or from the RF switch if so equipped. The tuning voltage for the tuner is developed from the frequency synthesis II06 mounted in the tuner. Band switching is performed by the B1 through B3 lines generated from II06. The output of the tuning section is the Video IF frequency of 45.75 MHz at pin 3 of the tuner.

RF AGC

The RF AGC control voltage is generated by the one-chip U1001 and is applied to the tuner at pin 1. The voltage at pin 1 controls the gain of the RF amplifier stages within the tuner. If a signal is weak, the AGC control voltage rises to increase the gain of the tuner. If the signal is strong, the control voltage decreases to lower the gain of the tuner to prevent overload. The AGC voltage range is about 2 volts DC for a strong signal to about 9 Volts for the weakest. The RF AGC control R2311 adjusts the operating range of the AGC control voltage. If the AGC control voltage does change when changing channels but the picture is always snowy, it is possible that the AGC stage within the tuner is defective and is not responding to the AGC correction voltage.

To verify operation of AGC stage within the tuner, connect a variable DC supply to pin 1 of the tuner. Tune the TV to a known strong signal. Set the DC supply to 2 VDC. The picture should be very snowy. Slowly raise the DC voltage up to a maximum of 9 VDC. The picture should clear as you raise the voltage. If not, the tuner may be defective.

Tuning Sequence

AFT, AFT REF, Sync Kill, and Tuning Sync

Three signals used during channel tuning are the AFT input, AFT Reference and Tuning Sync inputs to the system control micro U3101.

The AFT voltage developed in the one-chip is a voltage representation of the Video IF frequency. When the IF is equal to 45.75 MHz, the AFT voltage at pin 29 of the system control micro U3101 should be 2.5 VDC. This voltage is referred to as the AFT crossover point. If the local oscillator is set to the nominal tuning frequency and the received carrier is at nominal, the IF should be 45.75 MHz. Any AFT voltage above or below 2.5 VDC signifies that the received signal is not at nominal.

The AFT input at pin 37 of U3101 is converted from analog to digital information within U3101. During channel change, the DC voltage (5VDC) at pin 36 is read by U3101 to be used as a reference voltage for the AFT A/D converter. R3113 is attached to the 5 volt supply to establish the reference voltage. If R3113 opens, the A/D converter will not operate properly and produce AFT misallignment symptoms. This will give symptoms of misalligned AFT.

After the AFT reference is read, pin 36 of U3101 goes high during channel change to drive the sync kill line high. This turns on Pix Clamp Q3302 to apply 5 VDC to the sync kill line. The sync kill line is applied to the luma input of the one chip to bias it off, preventing noisy video from entering the sync separator during channel change and autoprogramming. This allows the horizontal oscillator in the one-chip to free run to produce a steady OSD.

The Tuning Sync input at U3101-12 informs the system control micro that an active channel is present. Horizontal sync is stripped from the video output of the one-chip and is applied to the system control micro. The positive going pulses are narrow and somewhat random. Note that the Tuning Sync input to U3101 is also a key scan output (KB3) used by the keyboard on the front of the set. When a key is pressed on the TV, the Tuning Sync input becomes a key scan output until the keyboard function is finished. If the channel up or down keys are pressed, the micro interrupts the key scan routine for about 10 milliseconds to perform a sync check at pin 12 to execute the tuning command. This sharing of functions was necessary due to the limited amount of input/output pins on the system control micro.

Air Tuning
When tuning an off-air channel, the system control micro sets the local oscillator in the tuner to 156 kHz above nominal for the channel being tuned. Then the AFT voltage is checked to see if it is less than 2 VDC. If it is, nominal minus 156 kHz is tuned. The AFT voltage is checked again to see if it is greater than 3 VDC. If it is, AFT crossover has been achieved and then the tuner is tuned to nominal.

If AFT crossover was not detected in the previous sequence, the tuner will be set to nominal plus 3.0 MHz and will decrement in steps of 0.5 MHz until AFT crossover is detected. Once AFT crossover is detected, the system checks for valid sync at the Tuner Sync input at U3101-12. If sync is detected, AFT is successively sampled to fine tune the channel. If AFT crossover is never detected, the tuner is set to nominal.

Once the channel has been tuned, AFT is no longer sampled and has no affect on the signal being received. AFT is only used during the initial tuning process.

Tuning Time - Air Mode
Nominal: 200 to 400 msec

Cable Tuning
The first step for cable channel tuning is the same as air tuning in that AFT crossover is checked by tuning 156 kHz above and below nominal. If AFT crossover is detected, a sync check is performed. If sync is present, the tuner is set to nominal.

If AFT was not detected or sync was not valid, the tuner is set to HRC (-1.25 MHz) plus 156 kHz. If the AFT voltage is less than 3 VDC, HRC minus 156 kHz is synthesised. If AFT is greater than 3 VDC, crossover is detected and a sync check is done. If sync is valid, the nominal HRC frequency is tuned.

If AFT crossover or sync was not detected in the HRC process in the previous paragraph, nominal plus 3.0 MHz is synthesised. Then the system begins to decrement the local oscillator in steps of 0.5 MHz until AFT crossover is detected. Once detected, a sync check is performed and AFT is fine tuned just as in air tuning mode. If sync was not detected at this point, the AFT crossover point is memorized. The system will then continue to decrement in 0.5 MHz steps in search of another AFT crossover with valid sync. If none is found, the previous crossover point is tuned. This gives the system capability to tune both offset music channels and offset scrambled channels which normally do not have valid video with the carrier.

Tuning Time - Cable Mode
Nominal: 200 to 400 msec
HRC: 300 to 500 msec
Music or Scrambled Channels: 1 to 1.5 sec

Note: HRC frequencies for channel 5 and 6 are different than other channels. The HRC frequency is +0.75 MHz instead of -1.25 MHz. The IRC frequency is +2.0 MHz. Both of these frequencies are checked when tuning channels 5 and 6 before the +3.0 MHz step is synthesised.

IF Defeat (TV PIX)

The TV PIX line at U3101-29 goes high when the TV tuner is the selected video source and goes low when an external input is being viewed. In sets without Pix-in-Pix, the TV pix line is tied to the pin 7 of U1001 to defeat the IF when an external input is being viewed on the screen. This keeps crosstalk for the TV tuner from entering the external video source. In sets with Pix-in-

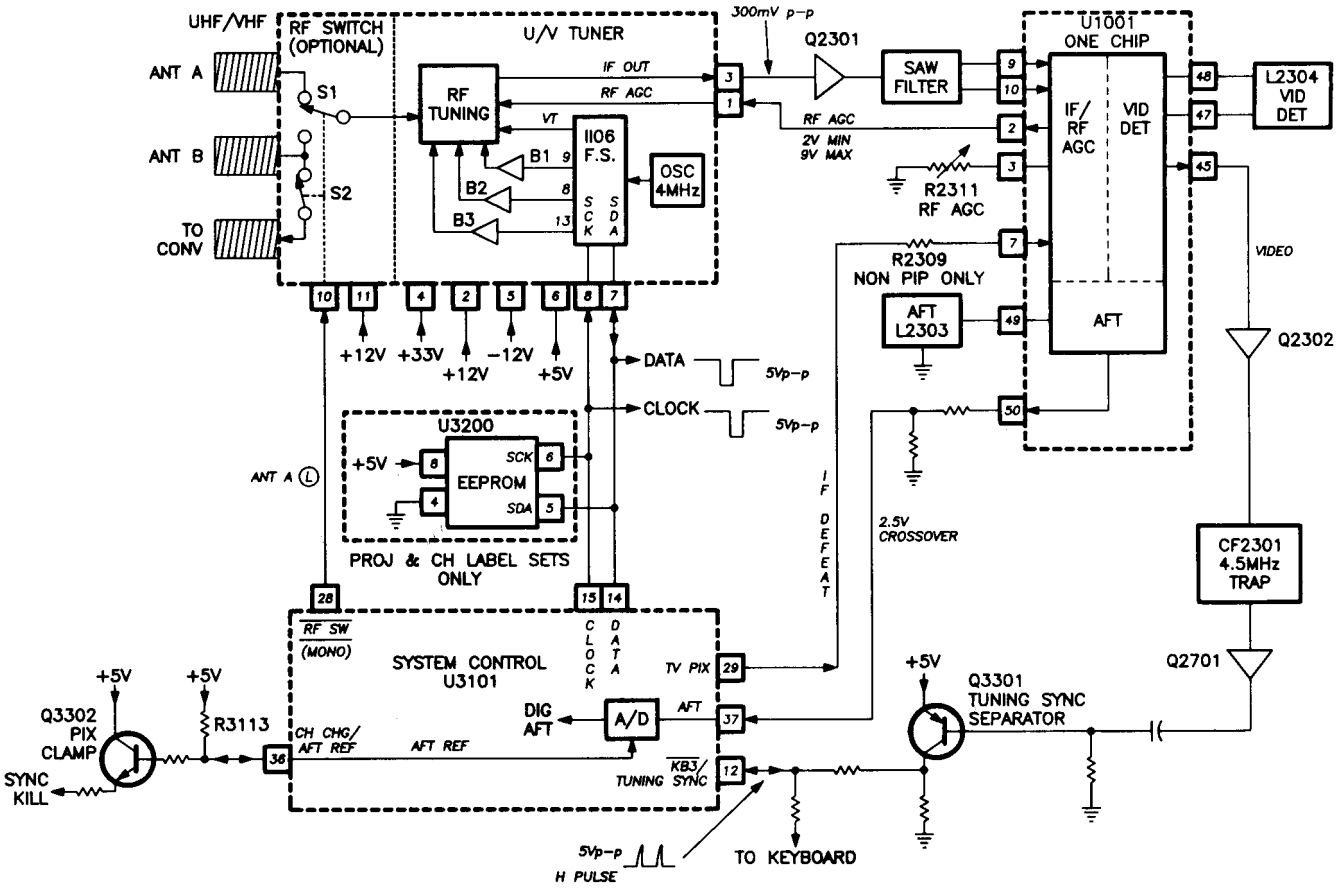


Fig. 13 Tuning Control (repeated)

Pix, the IF is not defeated when an external input is selected since the IF video may be used to fill the small pix when an external video source is in the big pix.

The TV PIX line is also used to bias the chroma input to the one-chip U1001. This is covered in the Luma and Chroma processing sections of this manual.

Power Supplies

If any or all of the +33, +12, and +5 volt supplies to the tuner are missing, the result will be a snowy picture with no video. The -12 VDC supply is used as a bias supply for band switch 2 and when missing shows very little effect on tuning except you may notice what appears to be a fine tuning problem on a few channels. Be sure to check all supplies to the tuner before assuming you have a tuner or IF problem.

Autoprogramming and EEPROM

All projection sets and direct view sets with the channel labeling feature contain a EEPROM (Electrically Erasable Programmable Read Only Memory) U3200. The EEPROM is a nonvolatile memory device which means it retains its stored information even when power is lost. It can also be altered to store new information unlike ROMs (Read Only Memory) whose data is permanent.

The following paragraphs list the tuning functions stored in the EEPROM. Refer to the system control section of this manual for other functions of the EEPROM.

Channel Scan List

Sets with EEPROMs installed will be programmed with channels 02 through 13 and CH 91 at the factory. The set will *not* automatically enter autoprogram mode when turned on after an extended power loss. Autoprogramming must be initiated by the setup menu.

Sets without the EEPROM will automatically enter autoprogramming mode when turned on after an extended loss of AC Power (coldstart). The autoprogram sequence can be initiated from the setup menu also.

The autoprogram sequence begins at cable channel 14 and checks for the presence of cable signals. If present, the system control micro keeps the tuner in cable mode and executes the autoprogram sequence. The AFT and sync check used during normal tuning as described earlier is also used during the autoprogram routine.

Alphanumeric Channel Labels

The four character alphanumeric label assigned to a channel by the customer is also stored in EEPROM. This feature is implemented only in sets with the EEPROM to prevent loss of this data.

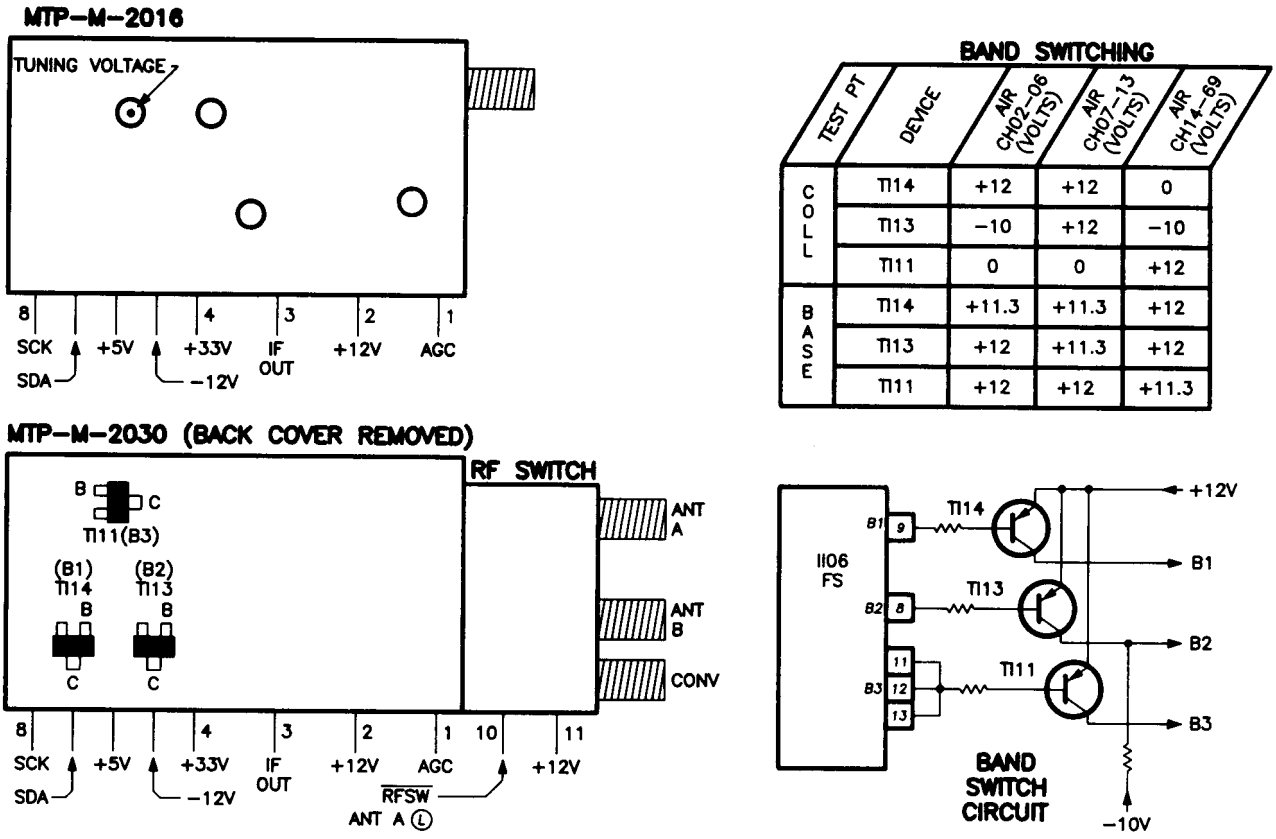


Fig. 14 Tuners/Band Switching

RF Switch Option and Menu Format
The EEPROM is programmed in the factory to tell the system control micro whether an RF switch is installed in the set. If the RF switch is not installed, the system control micro will delete the antenna selection feature from the setup menu.

Other feature variations such as Pix-in-Pix are also stored in EEPROM instead of using configuration code pins connected to the system control micro.

Clock and Data

All tuning commands are transferred to the tuner from the system control micro U3101 through the clock and data lines. Both lines are normally high with about four low going pulses per second when no buttons are pressed. The activity on the lines changes when any user control is accessed. Tuning troubleshooting is best done by checking for activity on the clock and data lines at the tuner connections. Interpretation of the data is nearly impossible.

Tuner Troubleshooting

Figure 14 shows the MTP-M-2016 and 2030 tuners. There are a few checks that can be made to determine whether the tuner is defective.

Note: Always check power supplies to the tuner before getting too involved in tuner troubleshooting.

1. Monitor the tuning voltage at the test point through the hole in the tuner shield as shown in figure 14. The tuning voltage should vary anywhere from 1 VDC to about 30 VDC while attempting to tune a channel. If it does change when you select various channels, you can be sure that the tuner is receiving commands from system control. If the voltage does not vary, connect a variable DC supply to the tuning voltage test point. Apply an RF signal to the tuner and select an active channel. Vary the DC supply from 0 to about 15 VDC. If you can see a picture being tuned as you vary the supply, the RF section of the tuner and the IF stages can be assumed good.
2. Verify that the band switches are operational. This is a difficult procedure because of the location of the band switching transistors. Figure 14 shows the band switching chart and the location of the band switch transistors on the tuner module. Select the air channels as shown in the chart and verify voltages on the base and collectors of transistors TI11, 13, and 14.

Tuning Problems

No Signal or Picture
If OSD responds to user channel change commands, Check Clock and Data lines going to tuner. If OK, perform tuning voltage verifications as described in step 1 above. If OK, check band switching as described in step 2 above. If OK, check for about 300 mV IF signal out of tuner pin 3.

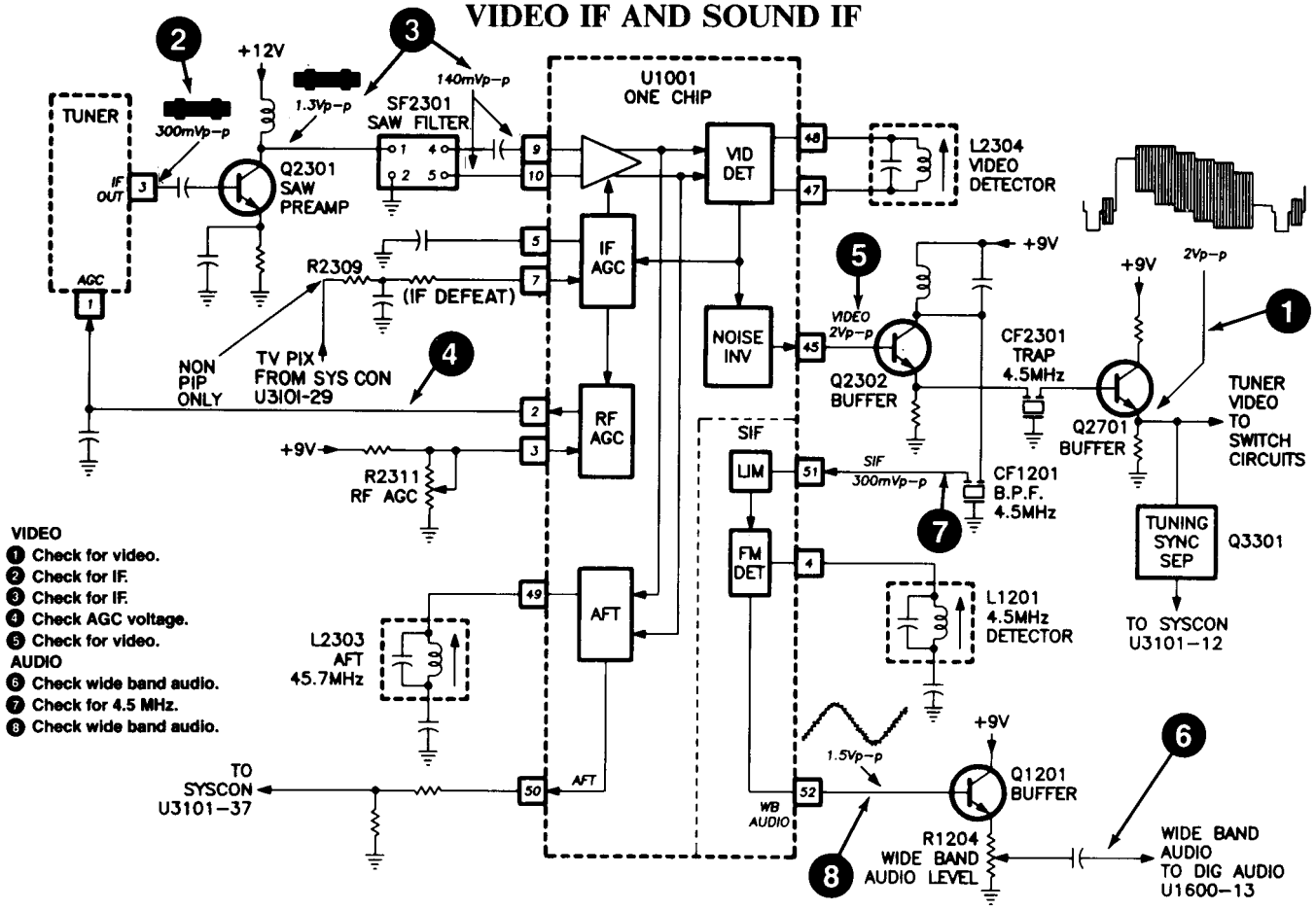


Fig. 15 Video IF/Sound IF

If OSD does not respond to user channel command inputs, suspect a system control problem.

Slow Tuning
If slow tuning occurs in cable mode but not air mode, check the tuning sync input to the system control micro U3101-12. You should see a high going pulse less than 8 μsec wide repeated at 68 μsec intervals. If tuning is slow in both cable and air modes, AFT alignment or the AFT reference voltage at U3101-36 needs verification. Check the circuits and align according to service data.

Drifting
If a channel is momentarily tuned and immediately drifts off frequency, suspect AFT alignment or AFT reference problems. Align according to service data.

Video IF

The 45.75 MHz IF signal exits the tuner at pin 3. The amplitude of the signal is about 300 mVp-p. The SAW preamp Q2301 amplifies the signal to compensate for losses in the SAW filter SF2301. The SAW filter used in the CTC168/169 chassis is of different composition than the ones used in the CTC157/159 chassis. The SAW used in the CTC168/169 has about an 800 ohm input impedance compared to 2500 ohms used in the CTC157/159 chassis in addition to 10 db less insertion loss. The key point to remember is that the two parts are not interchangeable.

The output of the SAW filter is applied to pins 9 and 10 of the one-chip U1001. The signal is amplified within the one-chip and is applied to the video detector. The output of the video detector is applied to the IF AGC stage which controls the gain of the IF amplifier.

The IF AGC control voltage is filtered by the capacitors on pins 5 and 7. The capacitor on pin 7 provides low frequency filtering while the capacitor on pin 5 provides high frequency filtering.

IF Defeat (TV PIX)
The TV PIX line from U3101-29 goes high when the TV tuner is the selected video source and goes low when an external input is being viewed. In sets without Pix-in-Pix , the TV pix line is tied to the pin 7 of U1001 to defeat the IF when an external input is being viewed on the screen. This keeps crosstalk for the TV tuner from entering the external video source. In sets with Pix-in-Pix, the IF is not defeated when an external input is selected since the IF video may be used to fill the small pix when an external video source is in the big pix.

RF AGC
The RF AGC control voltage is generated by the one-chip U1001 and is applied to the tuner at pin 1. The voltage at pin 1 controls the gain of the RF amplifier stages within the tuner. RF AGC is covered in more detail in the Tuning section of this manual.

AFT
The output of the IF amp within the one chip is also applied to the AFT stage. The output of the AFT stage varies from 0 to 9 VDC at pin 50 of the one-chip. A resistor divider network is used to scale the voltage down to 0 to 5 VDC at the AFT input at pin 37 of the system control micro U3101. With 4.5 VDC at U1001-50, 2.5 VDC should appear at U3101-37 to signify that the pix carrier is at 45.75 MHz. The role of AFT is covered in more detail in the Tuning section of this manual.

Video Detector
The video detector is a quasi-synchronous detector. The 45.75 MHz CW signal necessary for synchronous detection is derived from the 45.75 MHz AM signal by passing it through a limiter (to remove the AM) and the detector tank (L2304) which is a relatively high-Q BPF tuned to 45.75 MHz. The output of the video detector is applied to a noise inverter stage before exiting the one chip at pin 45. The amplitude of the video signal at pin 45 is about 2 Vp-p. The signal is buffered by Q2302. The signal at the collector of Q2302 is applied to the 4.5 MHz band pass filter CF1201 to pass only the 4.5 MHz audio signal. The signal at the emitter of Q2302 is applied to a 4.5 MHz trap to remove the 4.5 MHz audio information from the video signal. Q2701 buffers the signal to provide about 2 Vp-p to the video switching circuits and the Tuning Sync Separator circuit Q3301.

Sound IF

The 4.5 MHz band pass filter CF1201 passes only the 4.5 MHz sound IF signal to the sound limiter at pin 51 of the one-chip. The signal level is approximately 300 mVp-p. The output of the limiter is applied to the FM detector within the IC. The 4.5 MHz detector coil L1201 is adjusted to provide the maximum undistorted wide band audio output from the FM detector at pin 52 of the one chip. The signal at pin 52 is approximately 1.5 Vp-p depending upon the audio content. Q1201 buffers the wide band audio signal before application to the digital audio IC U1600-13. The amplitude of the wide band audio signal is adjusted by R1204. Note that this is not the volume control. Volume is controlled in the digital Audio IC U1600.

Video IF Troubleshooting

Symptom: No video, audio OK.
1. Since audio is taken from Q2302, the circuits prior to this stage must be OK. Check for video before and after the 4.5 MHz trap CF2301. If present, check for video at the emitter of Q2701. If present, the problem must lie beyond this circuit.

Symptom: No video or audio.
1. Check for video at the emitter of Q2701 and for audio at the emitter of Q1201 to verify if the problem lies in this stage. If neither is present, the problem must lie in this stage. If they were present, the problem lies beyond this point. Go to step 2.
2. Check for a 300 mVp-p IF signal at pin 3 of the tuner. If present, trace the signal through the SAW preamp and SAW filter to pins 9 and 10 of the one-chip. If present up to pin 9 and 10, go to step 3. If not present at pins 9 and 10, replace SAW preamp or SAW filter.
3. Check to see if the AGC line going to pin 1 of the tuner is greater than 2 VDC. If AGC voltage is 2 VDC, the gain of the tuner will be too low to receive a signal. If AGC is OK, go to step 4.
4. Make sure Video Detector is aligned according to service data. If alignment is OK, suspect a defective One chip.

AFT troubleshooting is covered in the tuner portion of this manual.

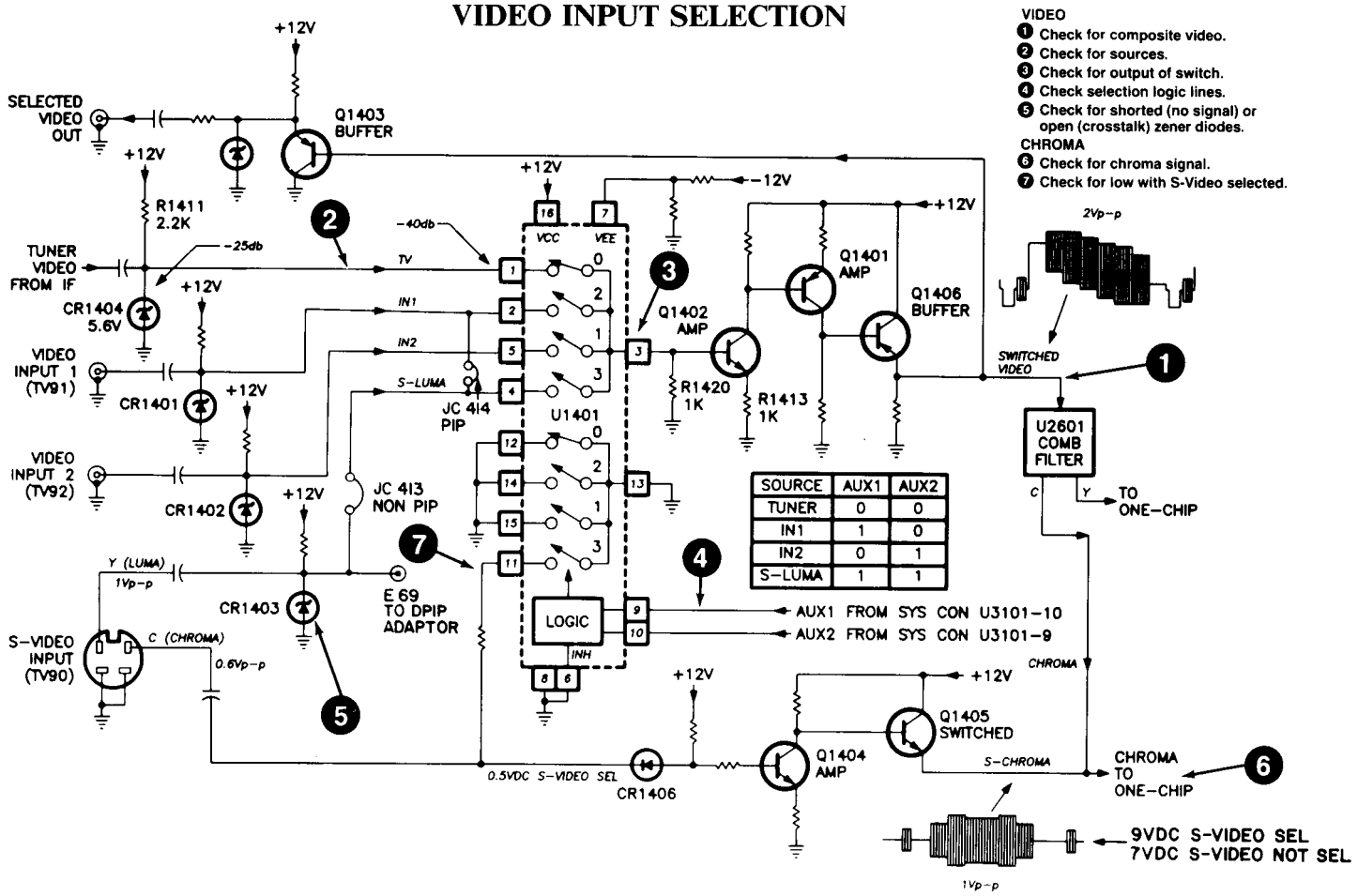


Fig. 16 Video Input Selection (Non PIP)

Figure 16 shows the video input selection circuit used in the CTC168/169. The S-Video selection shown in the figure is used in non PIP (Pix-in-Pix) sets with an analog comb filter. The digital comb filter uses a different S-Video selection technique which will be covered in the Digital Comb section of this manual. PIP sets with analog comb filters select S-Luma in a different manner which will be covered in a separate diagram.

Composite Video Inputs

The three composite video inputs to U1401 are Tuner, Input 1, and Input 2 video. The S-Luma signal from the S-Video connector is also switched by U1401 in non PIP sets. Two logic lines at pins 9 and 10 of U1401 select the desired video source. These lines originate from the system control micro U3101 and are labeled Aux 1 and Aux 2.

The chart in Figure 16 shows the logic states needed to select the three composite and the S-Luma signals. Note that there are two banks of four switches (0-3) in U1401. When switch 0 is closed in the upper portion, switch 0 is also closed in the lower portion. This also applies to switches 1 to 3.

ESD and Input Isolation

The 5.6 V zener diodes connected to all the video inputs are used for electrostatic discharge (ESD) protection and switching isolation which is not as obvious. Since all inputs are identical, the following explanation will use the TV Tuner input as an example.

When the Tuner Video is selected, switch 0 is closed in U1401. This allows R1411 and R1420 to form a voltage divider to bias pin 1 to about 4 VDC. The 5.6 V zener CR1404 doesn't conduct with only 4 volts on its cathode so it is essentially out of the circuit. The video signal goes unaltered except for the 4 VDC offset voltage.

When you select another video input, switch 0 opens. This removes R1420 from the circuit and allows R1411 to bias CR1404 into conduction. When the diode is conducting, its impedance drops enough to decrease the level of the video signal by about 25 db. The open switch 0 provides about -40 db isolation which is not enough isolation to prevent video crosstalk in the switch output. But add the -40 db isolation to the -25 db drop from the zener and you have an acceptable -65 db switch isolation. If one of the zener diodes opens, you will see two video sources on the TV screen if an active video signal is connected the input with the open diode. If a diode shorts, you'll loose the video signal it is attached to. This technique is used on all 4 switch inputs.

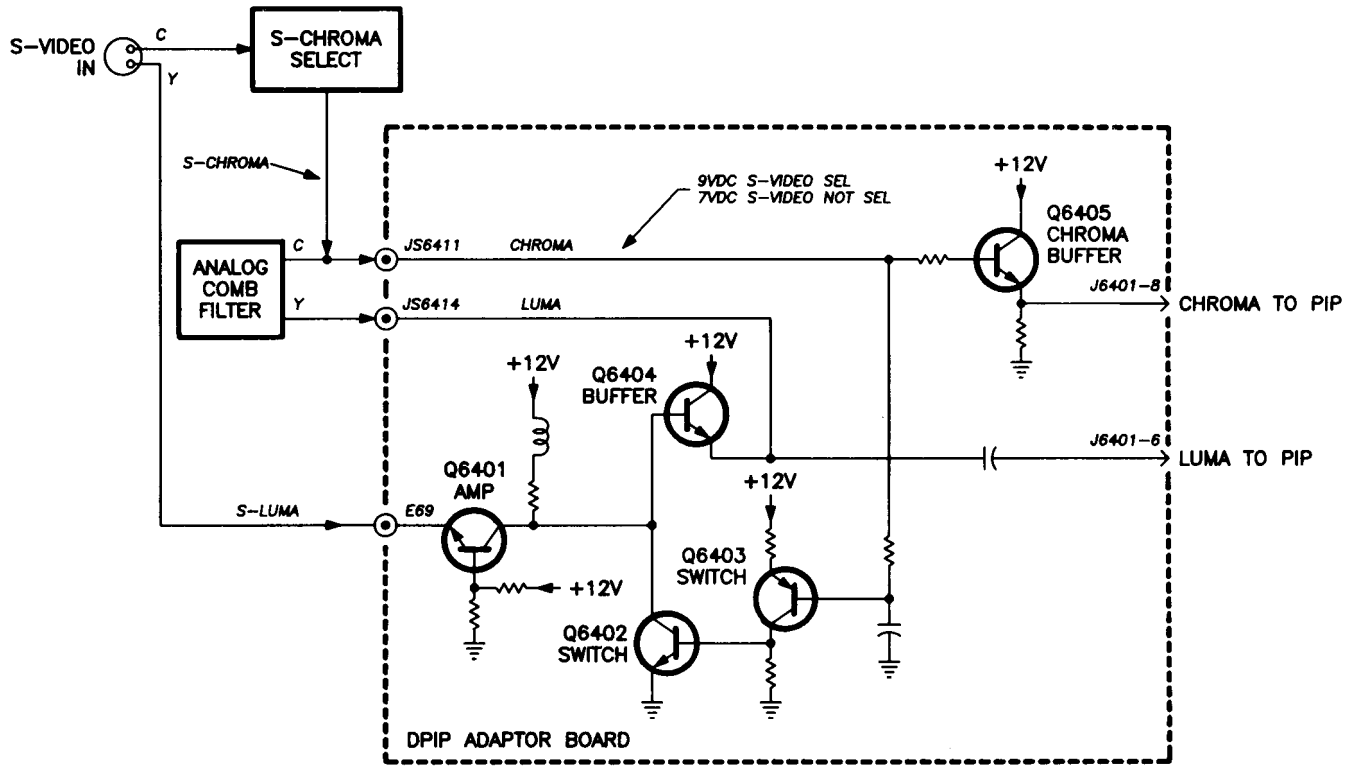


Fig. 17 S-Luma Selection With Analog Comb & PIP

Selected Video

The video output of U1401 at pin 3 is about 0.6 Vp-p (sync tip to white). The signal is inverted by by Q1402 and amplified to 2 Vp-p and inverted by Q1401. Q1406 buffers the signal to drive the comb filter and the selected video output buffer transistor Q1403. The output of Q1403 provides a video signal of 2 Vp-p unterminated (1 Vp-p terminated into 75 ohms) at the Selected Video Out jack on the back of the set. Note that the zener diode at the emitter of Q1403 is for ESD only and not signal attenuation as with the inputs of U1401.

S-Chroma Selection

The S-Luma signal is selected by switch 3 in the upper set of switches of U1401. S-Chroma is selected by using switch 3 of the lower half of U1401 to control the DC bias on the chroma signal.

Whenever S-Video is selected (TV channel 90), both switches labeled number 3 are closed. The lower switch at pin U1401-11 pulls the cathode of CR1406 low to turn it on. The DC voltage at the cathode is approximately 0.5 VDC when pin 11 is grounded through switch 3. The chroma signal then passes to the base of Q1404 where it is amplified to about 0.8 Vp-p at its collector. The chroma signal then passes through Q1405 and is applied to the chroma input of the one-chip. The chroma signal from the collector of Q1405 rides on a DC offset of about 9 volts whenever S-Chroma is selected. This DC offset will be used for S-Luma selection in analog comb PIP sets. This will be covered in the next section.

When any source other than S-Video is selected, the lower switch 3 is opened. This reverse biases CR1406 allowing Q1404 to saturate from its base bias. The collector of Q1404 goes low to turn off Q1405. With Q1405 off, the chroma signal from the comb filter is allowed to pass to the one-chip instead of the S-Chroma signal. The DC offset of the chroma signal from the comb is about 7 volts.

Input Selection Variations with PIP

The S-Luma selection shown in figure 16 is used for non PIP sets. JC413 passes the S-Luma signal to U1401 and JC414 is not installed in non PIP sets. In sets with PIP and analog comb filters, JC413 is omitted and JC414 is added. Since JC413 is omitted, the S-Luma signal is routed to the DPIP adaptor board from point E69. The DPIP adaptor board performs the S-Luma selection.

With JC414 installed in PIP sets, the composite video from input one will be selected by U1401 whenever S-Video is selected.

S-Luma Selection with Analog Comb and PIP

Figure 17 shows how S-Luma is selected in sets with an analog comb and Pix-in-Pix. The circuit shown in the dashed box is contained on the DPIP adaptor board whose main function is to provide signals to and from the PIP module. The only active circuits on the board are shown in figure 17 while the rest of the board is merely signal routing to connectors. Refer to service data for a detailed schematic for the signals going to and from the DPIP adaptor board. The DPIP adaptor board is replaced by the video features SIP board in digital comb sets. Connectors on the video features board deliver signals to and from the PIP module.

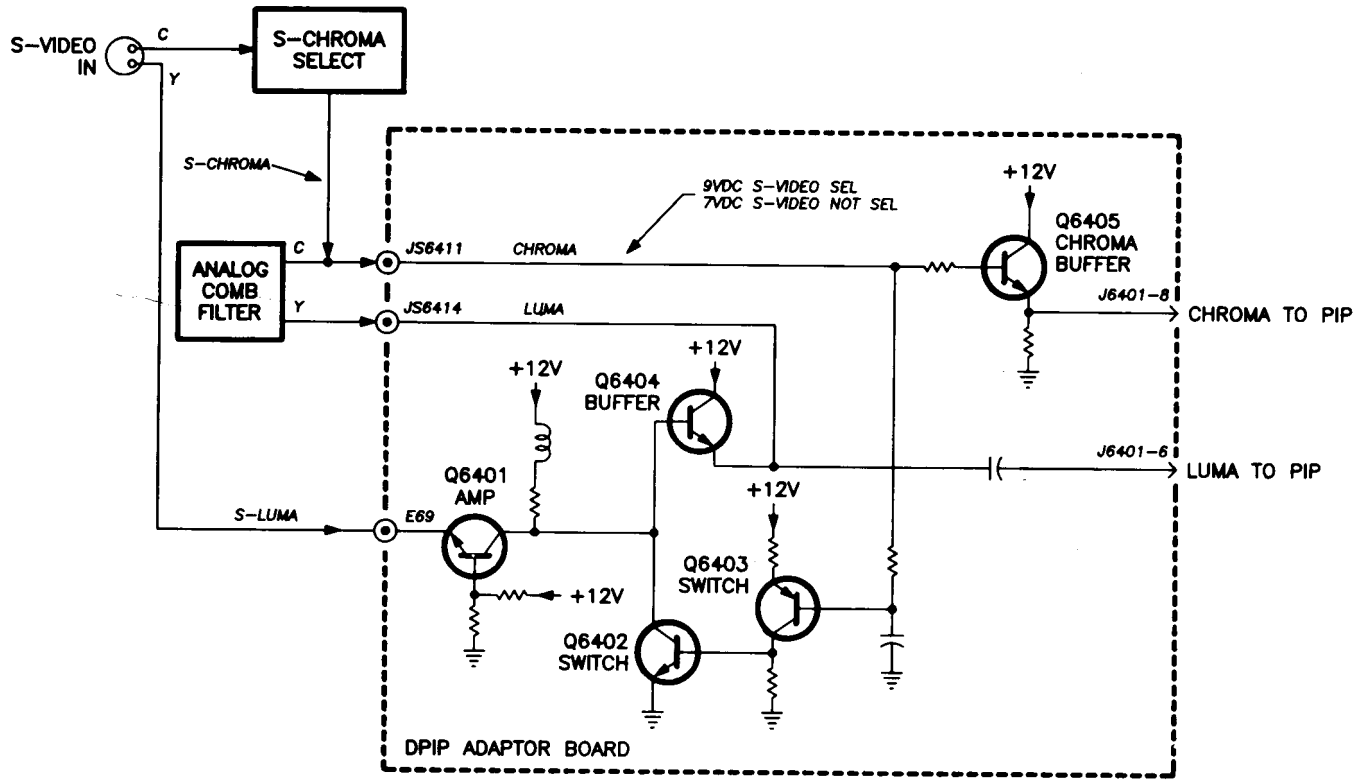


Fig. 17 S-Luma Selection With Analog Comb & PIP (repeated)

S-Luma Selection using Chroma DC Offset
The Y and C signals from the analog comb enter the DPIP adaptor board at JS6414 and JS6411. The S-Chroma signal is also connected to the comb chroma signal and is selected as described in figure 16. The Chroma signal is buffered by Q6405 and passed to the PIP module. The chroma signal is also applied to the base of Q6403. More about this later.

The S-Luma signal enters the adaptor board at E69 and is applied to amp Q6401. The luma signal from the comb is attached to the emitter of Q6404 and capacitively coupled to the PIP module. Whenever S-Chroma is selected, the DC offset on the chroma line is about 9 VDC. This DC voltage biases Q6403 off which turns Q6402 off. Since Q6402 is off, the luma signal from the collector of Q6401 is buffered by Q6404 and is applied to the luma input of the PIP module. The DC offset from the emitter of Q6404 turns off the luma output of the comb to allow only the S-Luma signal in the output.

When S-Chroma is not selected, the DC offset on the chroma line is about 7 VDC. This offset is low enough to turn on Q6403 which also turns on Q6402. Q6402 pulls the base of Q6404 low and turns it off allowing only the luma signal from the comb to pass to the PIP luma input.

Video Input Selection Troubleshooting

Non PIP Sets

Symptom: No video.
1. Check for composite video at the emitter of Q1406. If present, the problem must lie beyond this point. If not present, check for video at input of selection IC. If present, check logic levels at pins 9 and 10 according to chart in figure 16. If OK, check for shorted zener diodes at inputs of U1401.

Symptom: Two video sources on screen.
1. Check for open zener diodes at inputs of U1401.

Symptom: Chroma distorted or missing.
1. With S-Video selected, check for low at U1404-11. If not low, S-Chroma will not be selected. Trace chroma signal through Q1401 to Q1405.
2. With composite video selected, make sure Q1405 is turned off and check for chroma signal from comb filter.

PIP Sets with Analog Comb

Symptom: No video.
1. Check for Y and C signals at input of PIP module or at output of DPIP Adaptor board. If present, refer to PIP module troubleshooting in later section of this manual. If no Y/C signals at output of DPIP adaptor board, go to step 2.
2. Check for Y and C signals from comb at input of DPIP adaptor board at JS6411 and JS6414. If not present, check comb filter. If present go to step 3.
3. Trace chroma signal to buffer Q6405. Also check for DC offset on chroma line as shown in figure 17. Check operation of switch transistors Q6403 and Q6402. Check Luma Amp Q6401 and Buffer Q6404.

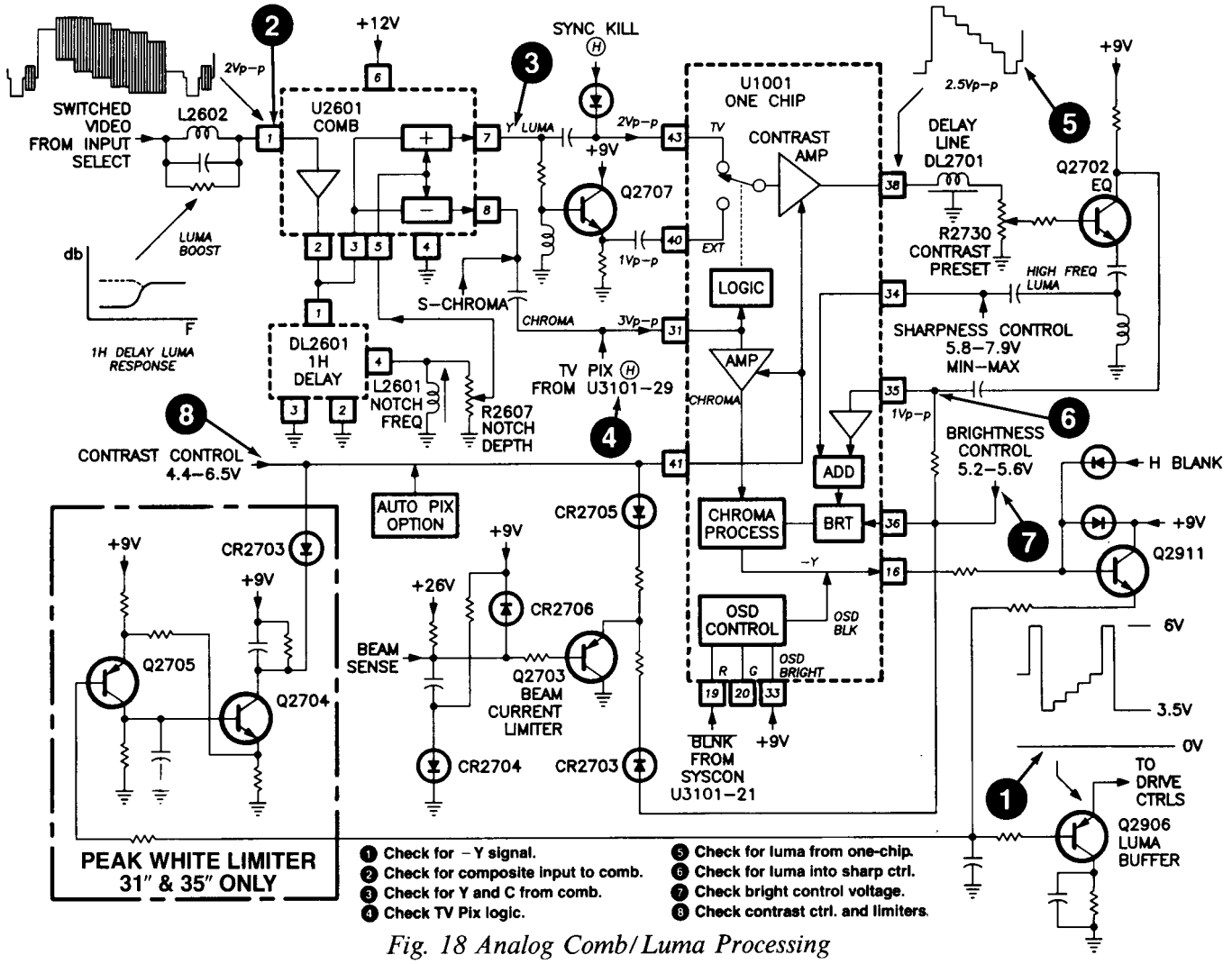


Fig. 18 Analog Comb/Luma Processing

The composite video signal from the input selection stage is applied to pin 1 of the comb filter U2601. The LC network at pin 1 is used to compensate for the loss of low end frequency response introduced by the glass delay line DL2601. The composite signal is buffered within U2601 for application to the 1H delay line and to the comb input at pin 3.

The composite video signal is applied to an adder and subtractor circuit within U2601. The 1H delayed signal is also applied to both the adder and subtractor. The resulting signal from the adder is the luminance (actually 2Y) signal while the chrominance signal (2C) is developed from the subtractor.

The output of the 1H delay line is applied to the notch frequency L2601 and notch depth control R2607. The notch frequency peaks the signal at the proper frequency while the depth control applies the proper amplitude for the cancellation effect within U2601.

Luma Selection

The luma output of the comb filter is applied to pin 43 of the U1001 and also to the base of Q2707. The inductor in the base of Q2707 provides added peaking to provide the extra bandwidth for the S-Luma signal. The peaked signal is buffered by Q2707 for application to U1001-40. The signal is reduced to 1 Vp-p for the one chip at pin 40 as opposed to 2 Vp-p at pin 43.

The TV Pix line from the system control micro is used to select between the two luma inputs of the one-chip. When the TV tuner is selected, the TV PIX line goes high to raise the DC bias at pin 31 (also the chroma input) to about 4.5 VDC. This is sensed by the internal logic circuit in U1001 to select the luma signal at pin 43. When an external video input is selected, the TV Pix line goes low to lower the DC bias on pin 31 at 1.2 VDC. This causes the logic circuit to select the luma signal at pin 40.

Sync Kill

During channel change and autoprogramming, the sync kill line goes high to prevent noisy luma signals from entering the sync separator. This prevents tearing and instability in the OSD display during channel change and autoprogramming.

The sync kill action is achieved by raising the DC offset of the luma signal into U1001 at pin 43. With sync kill

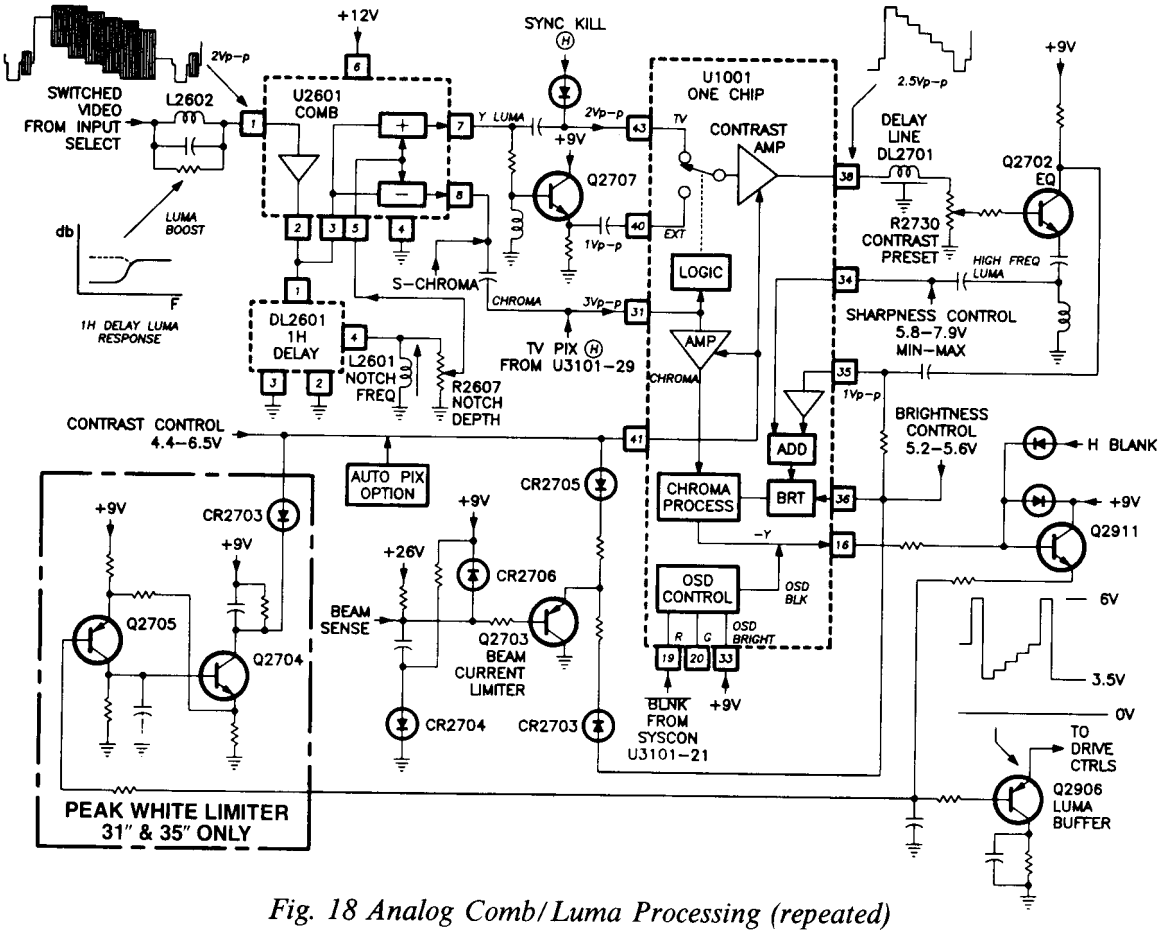


Fig. 18 Analog Comb/Luma Processing (repeated)

off, the DC offset at pin 43 is about 3 VDC. With sync kill on, the DC offset raises to about 5 VDC which biases off the input of the contrast amp within U1001.

Contrast Control

The luma signal from either pin 43 or 40 is applied to a voltage controlled contrast amp. The contrast control at pin 41 of U1001 affects the peak to peak amplitude of the luma signal from the contrast amp at pin 38. Also note that the contrast control affects the chroma amp within U1001. This will be covered in more detail in the chroma section of this manual. The DC control is derived from filtering the PWM output from the system control micro. The range is about 4.4 to 6.5 VDC going from min to max contrast.

Beam Current Limiter

To prevent blooming on extremely bright scenes, the beam current limiting circuit pulls the contrast and brightness controls down to decrease the beam current.

When beam current increases, the beam sense voltage at the base of Q2703 decreases. This turns on Q2703 and decreases the voltage on the contrast control through CR2705 and the voltage on the brightness control through CR2703.

Peak White Limiter

The peak white limiter which may be used in the 31" and 35" chassis acts in a similar manner as the beam current limiter except faster. The peak white limiter can respond quickly to peaks in the luma signal instead of relatively slow changes in beam current.

Q2705 conducts during white peaks of the -Y signal. This applies voltage to the base of Q2704 turning it on to pull the contrast control lower. This prevents shadow mask warpage from the localized high beam currents for the peaks of the -Y signal.

Auto Pix

The auto pix circuit is built onto the video features sip and is covered in that section of this manual. It too pulls down the contrast control according to scene content.

Sharpness Control

The luma signal from pin 38 of U1001 passes through a delay line DL2701 to compensate for chroma processing delays. The delay line output is applied to the contrast preset control R2730. Q2702 equalizes the signal and provides high and low frequency luminance signals for the sharpness control circuit.

The high frequency components of the luma signal from the emitter of Q2702 are applied to pin 34 of the one chip while the low frequency components from the collector are applied to pin 35. Both signals are applied to an adder circuit within U1001. The DC voltage form the sharpness control applied to pin 34 of U1001 determines how much of the high frequency luma signals are added to the final luma signal. At minimum sharpness, about

5.8 VDC at pin 34, little if any high frequency luminance is added while all is added at maximum sharpness (7.9 VDC). The output of the sharpness adder is applied to the brightness control circuit.

Brightness Control

The luminance signal from the sharpness control is applied to the brightness control circuit which is controlled by a DC voltage at pin 36 of U1001. At minimum brightness, about 5.2 VDC is applied to pin 36 and about 5.6 VDC at maximum. The brightness control lowers the DC offset voltage of the luminance signal to obtain higher brightness and raises the offset voltage to produce a darker picture. When checking the brightness control voltage, remember that it can be pulled down by the beam current limiter during very bright scenes.

The output of the brightness control is applied to the chroma processing stage for R, G, and B-Y processing. It is also inverted in the chroma stage to create the -Y signal at pin 16. The horizontal blanking pulse is added to the -Y signal from a pulse from the flyback. The -Y signal is buffered by Q2911 and Q2906 for application to the CRT driver stages.

OSD Black Surround and Blanking

The BLNK signal from the system control micro at pin 19 of U1001 is used to create the black border around the OSD characters and blank the luminance signal during channel change. Normally pins 19 and 20 are used for adding OSD information to the video signal. In this application, pin 19 is used only for blanking and character black surround.

When pin 19 is pulled low, the voltage at the OSD Bright input at pin 33 is a transferred to the -Y signal. Since the voltage at pin 33 is +9 VDC, the -Y signal is blanked. Whenever a character is displayed on the screen, low going pulses can be viewed on pin 19. During channel change, pin 19 goes low for the duration of tuning followed by pulses until the OSD channel indicator times out.

Note: If the -Y signal at U1001-16 contains blanking only with no luma information, make sure pin 19 of U1001 is not stuck low before diagnosing U1001 as being defective.

Luma Processing Troubleshooting

Symptom: No video.

1. Check for -Y signal at emitter of Q2906. If present, the problem lies beyond this point. If not present go to step 2.
2. Check for composite video input at pin 1 of the comb filter U2601. Trace composite signal from pin 2 and 3 of U2601 through 1H delay line to pin 5. Check for Y and C signals from comb. If present, go to step 3.
3. Check for luma at pins 43 and 40 of U1001. Make sure Sync Kill line is not active except during channel change. Check TV Pix control bias at pin 31. If OK, go to step 4.
4. Trace luma signal from U1001-38 to pin 35. Check brightness and contrast controls and associated limiting circuits. Make sure U1001-19 is not stuck low.

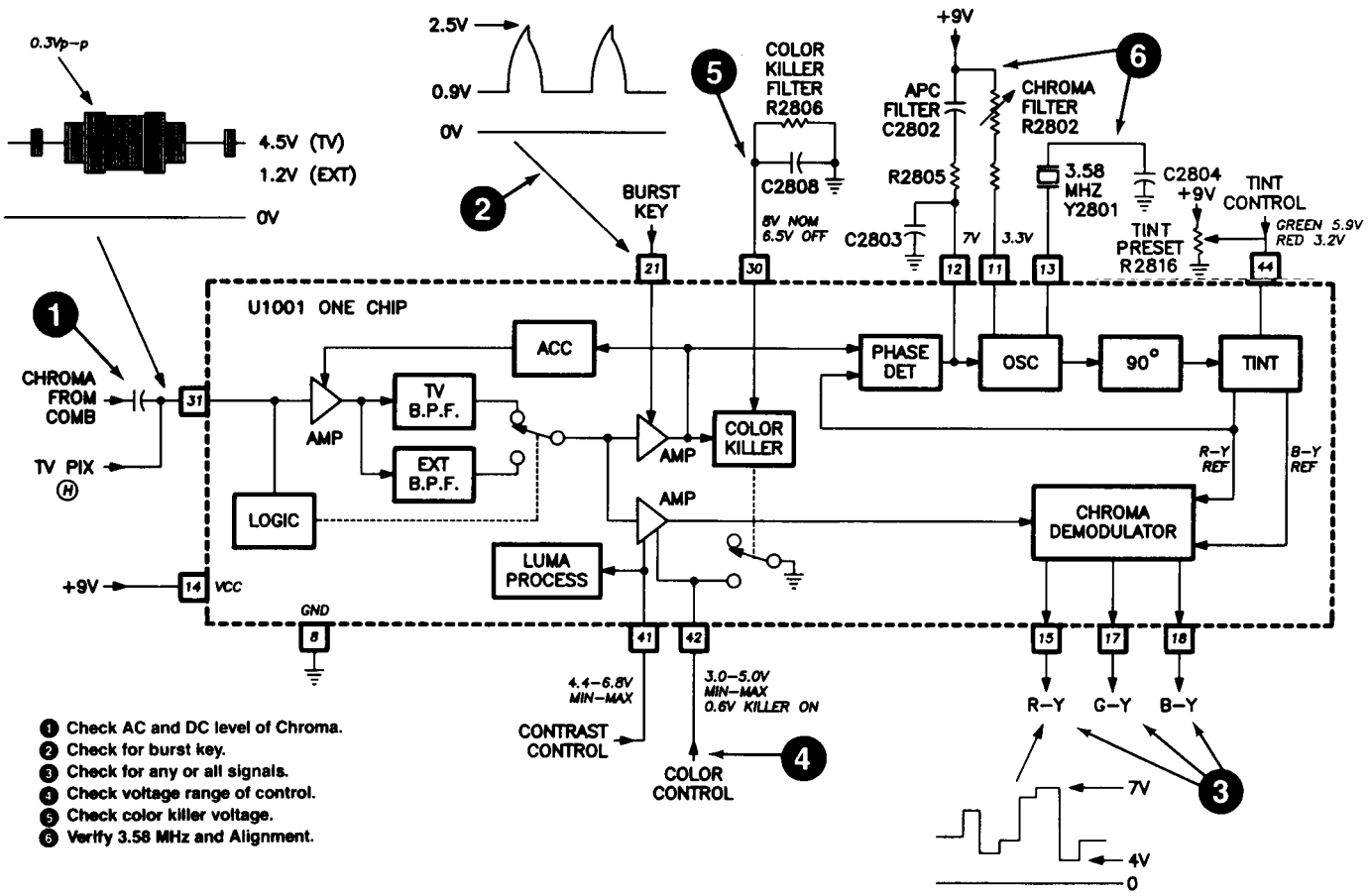


Fig. 19 Chroma Processing

The chroma signal from the comb filter enters the one-chip U1001 at pin 31. The DC offset of the chroma signal at this point determines which chroma band pass filter is selected within U1001. The TV Pix line from system control shifts the offset at pin 31 to perform the internal switching.

With the TV tuner selected, the TV Pix line is high to place about 4.5 VDC DC offset at pin 31. The logic circuit within U1001 detects the offset and selects the TV band pass filter. When an external video signal is selected, the TV Pix line goes low and the DC offset at pin 31 goes to about 1.2 VDC. Then the logic stage selects the external band pass with different amplitude characteristics than the TV band pass.

The ACC control monitors the chroma burst level and adjusts the gain of the chroma amp after pin 31 to maintain a constant chroma level.

Burst Key

The output of the switch is applied to a keyed amp which is on only during horizontal blanking. The keying pulse supplied from deflection is applied to pin 21 of U1001. This pulse is also used as a feedback pulse for the horizontal AFC stages. Loss of this signal will create no chroma symptoms as well as horizontal tearing on the screen.

Color/Contrast and Tint Controls

All three parameters are controlled by filtered PWM signals from the system control micro U3101.

Color/Contrast

The color level control at pin 42 varies the level or saturation of the demodulated chroma signal viewed on the screen. Minimum color is obtained at about 3 VDC at pin 42 and maximum at about 5 VDC. When the color killer circuit is activated, the voltage at pin 42 is pulled to about 0.6 VDC by an internal switch within U1001.

The contrast control is also tied to the chroma amp to allow the chroma level to track the luma level. When the contrast goes up or down, so does the chroma level.

Tint

The tint control alters the chroma demodulation circuit to alter the hue or tint of the demodulated chroma signal. The red end of the tint range is achieved at about 3.2 VDC at pin 44 while the green end occurs at 5.9 VDC. The tint preset control R2816 allows you to alter the tint setting obtained from the picture reset feature.

Color Killer

The color killer pulls the color control at pin 42 to about 0.6 VDC when either the color burst is not present or at

extremely low levels. The voltage developed on the killer filter at pin 30 determines the color killer activation point. With color burst present, the voltage at pin 30 is about 8 VDC. If the voltage drops to about 6.5 VDC, the color killer activates to turn the chroma circuits off to prevent chroma noise in the picture.

Chroma APC

The chroma APC filter at pin 12 provides accurate tracking of the color burst phase which is at 180 degrees reference. The DC voltage at pin 11 is normally about 7 VDC. If the APC filter cap C2802 is decreases in value due to age, horizontal bars in the chroma signal will result. If C2803 shorts, chroma will be lost.

Chroma Filter and Oscillator

The chroma filter adjustment R2802 aligns internal chroma filters within U1001 in addition to adjusting the 3.58 MHz oscillator at pin 13. If not adjusted properly, chroma phase (tint) may be shifted or loss of chroma may result. Refer to service data for the alignment procedure.

To measure the chroma oscillator frequency without introducing probe capacitance error, force the tint control at pin 44 of U1001 to about 1.3 VDC. The oscillator frequency can be measured at the B-Y output at pin 18 of U1001. It is not necessary to follow this procedure just to verify that the oscillator is running, but only when you need a precise frequency measurement.

Chroma Troubleshooting

Since most problems in the chroma stages result in loss of chroma, DC voltage and signal verification is the best way to troubleshoot this stage.

1. Check for R, G, or B-Y outputs at pins 15, 17, and 18. If not present, check for chroma input as well as DC offset at pin 31.
2. Check for burst key at pin 21.
3. Check color killer voltage at pin 30.
4. Check for leaky or open APC Filter C2802 at pin 12 Also check the 3.58 MHz oscillator.

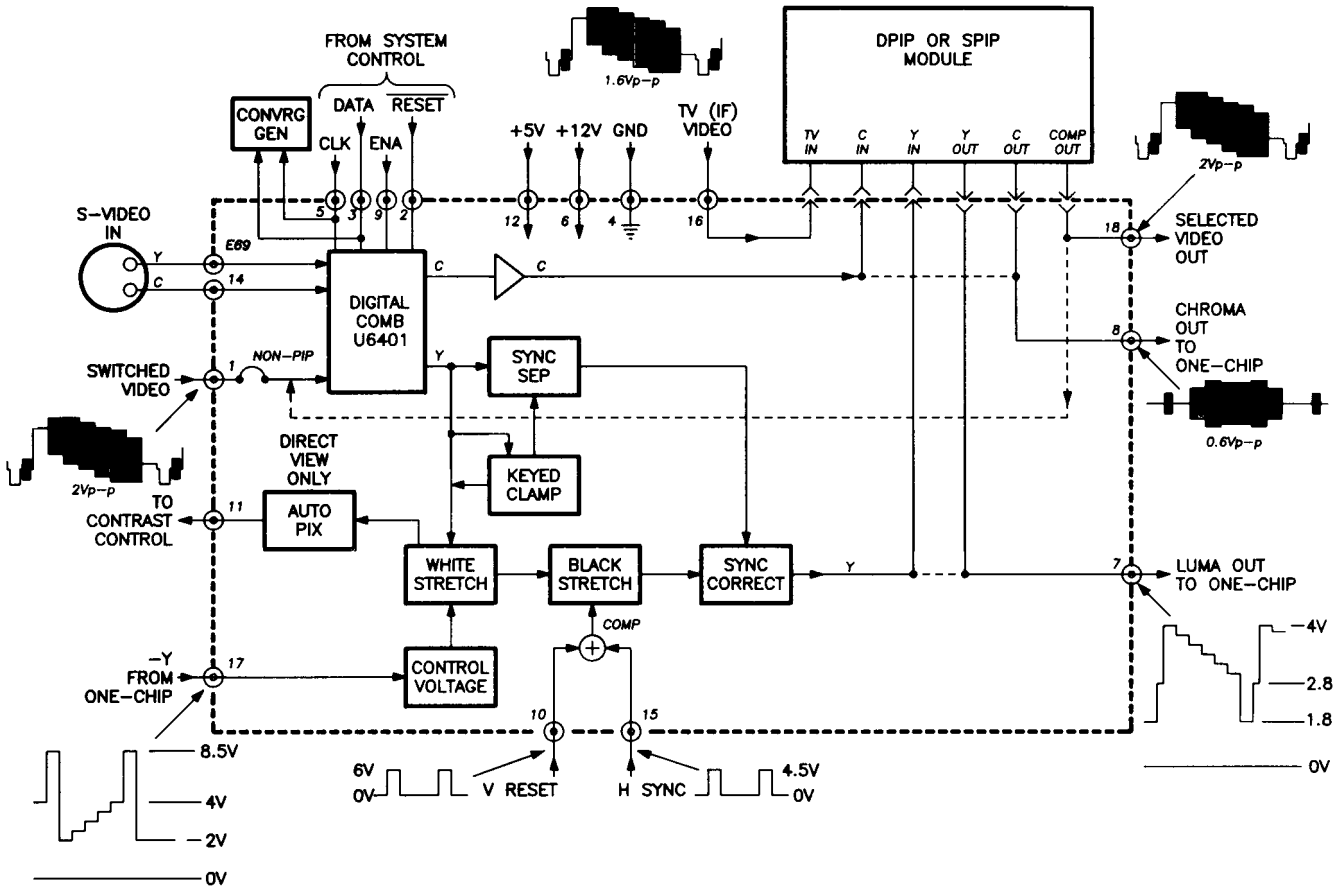


Fig. 20 Video Features SIP

Figure 20 shows a block diagram of the video features sip which is used in some versions of the CTC168/169. The features contained on this board are Digital Comb Filter, White and Black Stretch, Auto Pix, and Pix-In-Pix interface. These circuits will be covered in detail in the following sections of this manual.

Signal Flow

While figure 20 does not show every possible interconnection scheme for all the chassis variations, it does show the key signals going to and from the module. In cases such as Pix-In-Pix, some of the signals may be routed differently through the module than shown here. Refer to service data for all possible interconnect schemes.

Since gaining access to the back of the video features sip is difficult, it is best to verify signals at the pins of the sip to quickly determine if the module is at fault. If the sip is producing a luma and chroma signal at pins 7 and 8, the module is probably OK.

Composite and S-Video Selection

The start of the signal chain begins at the digital comb filter which takes the composite video signal at pin 1 and separates it the luma (Y) and chroma (C) signals. The signal at pin 1 comes from the video selection circuit in non PIP sets. In PIP sets, the input comes from the Comp Out of the PIP module. Again this will be covered later.

The digital comb also selects the Y/C signals from the S-Video connector from the back of the set. The digital comb is used only as a selection device for the S-Video signals and does not comb or process them.

The digital comb receives its switching and gain commands through serial communications bus at pins 2, 3, 5, and 9.

Chroma Path

The chroma output of the digital comb takes one of two paths. Without PIP, chroma from the comb is sent directly to pin 8 of the Video Features sip for application to the one-chip. With PIP, the chroma signal is applied to the chroma input of the PIP module. The chroma output of the PIP module enters the SIP for application to the chassis.

Luma Path

The luminance output of the digital comb is applied to a sync separator, a clamp circuit, and finally to the white stretch circuit. The output of the white stretch circuit enters the black stretch stage. The output of the black stretch stage is sync corrected and passed to pin 7 of the SIP if PIP is not installed. If PIP is installed, the luma signal is applied to the PIP luma input. The PIP luma

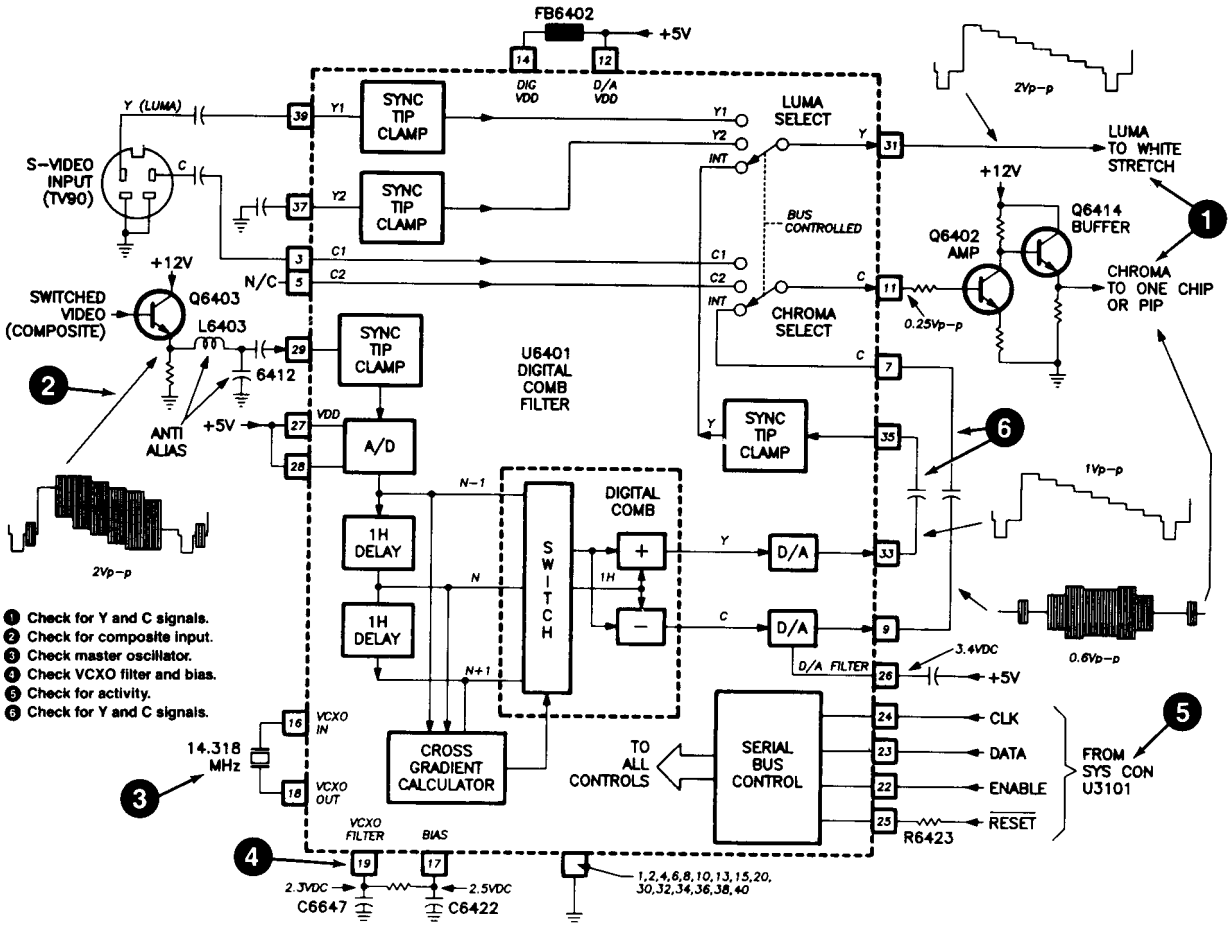


Fig. 21 Digital Comb Filter

output is then applied to pin 7 of the features sip for application to the one chip.

TV(IF) Video - Pin 16

The PIP module requires the TV tuner video source for its selection circuits. The tuner video is routed through the video features sip from pin 16 to the pip module.

Selected Video Out

The composite video signal (Comp Out) from the video selection circuits within the PIP module is routed through the video features sip to pin 18. The signal is routed from pin 18 to the Selected Video Out jack on the back of the set. The signal is also routed to the input of the digital comb. This signal path will become more apparent after reading the PIP portion of this manual.

Auto Pix and -Y

The Auto Pix circuit monitors the -Y luminance signal at pin 17 and pulls the contrast control at pin 11 lower to prevent blooming on the screen. This circuit is only implemented in direct view sets.

H and V Inputs

The clamp circuit in the black stretch stage requires composite blanking to operate. The vertical reset signal at pin 10 is summed with the H sync signal at pin 15 to produce composite blanking.

Digital Comb Filter

The Digital comb filter is mounted on the video features SIP to provide Luma/Chroma separation and S-Video input switching. The digital comb eliminates hanging dots on vertical color transitions in the picture. A color bar pattern on the top half of the screen and red on the bottom of the screen is an example of where hanging dots would appear. You would see a jagged pattern at the transition of the color bars to the red half of the screen on a conventional comb filter. When the color content changes between the top and bottom halves of the screen, so does the chroma phase from one horizontal line to the next resulting in incomplete chroma cancellation in the comb.

The switched video input from the chassis U1401 or from the PIP module is buffered by Q6403. The LC network in the emitter is needed to limit the high frequency content of the video signal to prevent alias frequencies from being formed with the sampling frequency within comb. The video signal passes through a sync tip clamp to the analog to digital converter. The output of the D/A is called the N-1 signal. This a applied to the switching input of the digital comb and also to a 1H delay circuit. The output of the 1H delay is labeled N and is applied to the switch and to another 1H delay. The output of the final 1H delay is called N+1 and is applied to the switch.

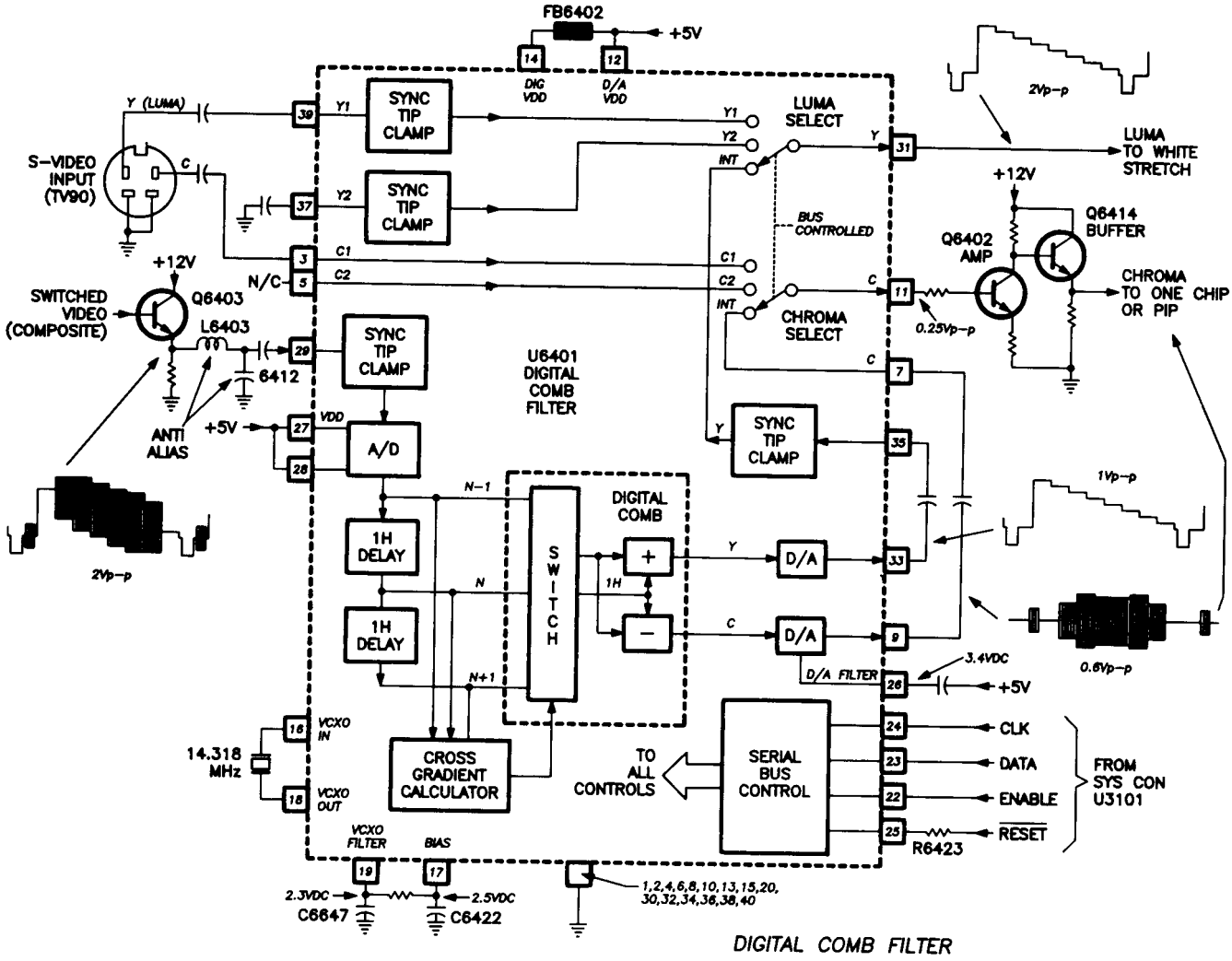


Fig. 21 Digital Comb Filter (repeated)

All three signals (N-1, N, and N+1) are applied to the cross gradient detector which senses which two signals contain about the same video content. The output of the calculator is applied to the switch to select the most similar video signals for application to the comb. This will create the best cancellation effects of the luma and chroma signals and reduce or eliminate the hanging dot effect.

The Y and C outputs of the digital comb stage is converted from digital to analog signals and exit the IC at pins 33 and 9. The D/A filter voltage at pin 26 operates at about 3.4 VDC. This voltage controls the current in the D/A circuit. The Y and C signals are capacitively coupled back into the IC at pins 35 and 7. The luma signal goes through a sync tip clamp to the luma select switch. The chroma signal is applied directly to the chroma select switch.

The other two inputs the luma and chroma select switches are the Y and C signals from the S-Video connector.

There are provisions on the IC for two S-Video connectors but only one is utilized. The Y and C switches are controlled by the serial bus control circuit within the IC.

There are no individual logic pins on the IC to control the switch positions. The selected luma signal exits at pin 31 and is applied to the white stretch circuit. The chroma signal exits at pin 11 and is amplified by Q6402 to about 0.6 Vp-p and buffered by Q6414. The buffered chroma signal is either applied directly to the one-chip or to the PIP module if available.

Serial Communications Bus

All internal switching commands within the digital comb are bus controlled by the serial bus lines at pins 22, 23, and 24. The Reset line at pin 25 is a very sensitive input and should not be probed directly at the pin. Check on the other side of R6423 for the proper logic level of the reset line. Placing a probe on pin 25 does no electrical damage, but it will reset the digital comb which will give you a blank screen until the set is tuner off and back on.

Video parameter settings within the digital comb such as luma level and chroma phase are initialized over the serial communications bus from the system control micro U3101. The values for the settings are stored in the EEPROM. For this reason, all sets containing a digital comb must also contain a EEPROM.

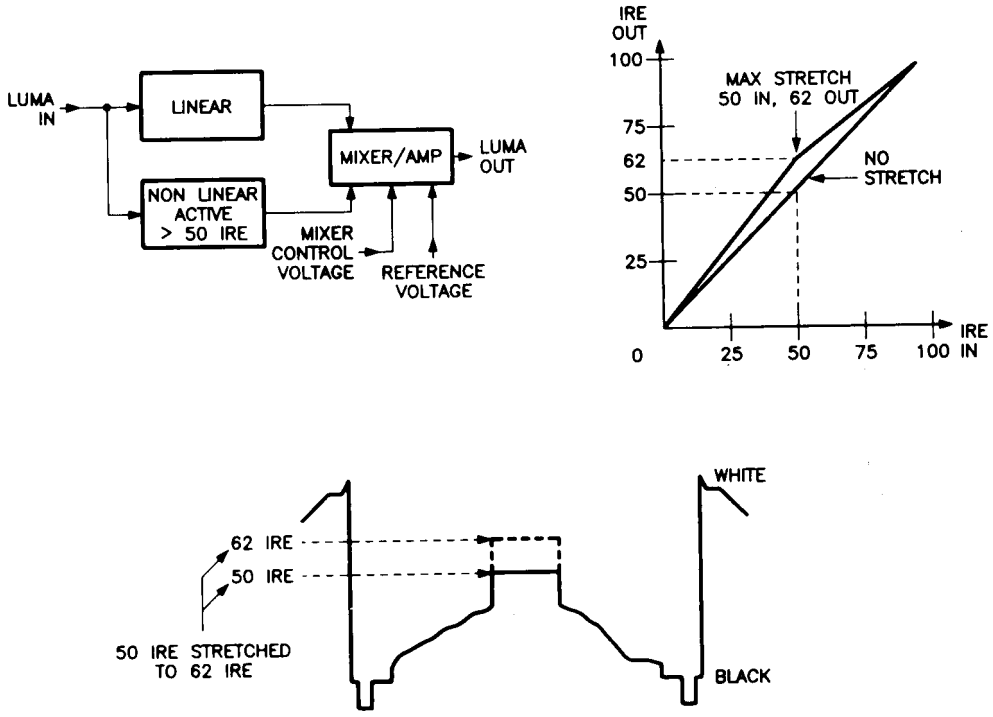


Fig. 22 White Stretch Operation

VCXO

The digital comb contains a voltage controlled oscillator that runs at 14.318 MHz. The bias for the VCO is approximately 2.5 VDC and is supplied by pin 17. The filter at pin 19 runs at about 2.3 VDC. Unlike the reset pin 25, all three of these pins may be probed when troubleshooting.

Digital Comb Troubleshooting

Symptom: No Video.

1. Check for luma and chroma signals at U6401-33 and 11. If present, the problem lies beyond the digital comb. If No signals are present, go to step 2.
2. Check for composite video at input pin 29. If missing, the problem lies prior to digital comb. If signal is present, go to step 3.
3. Check for Y and C signals at pins and 33 and 9. If present, check for Y and C at pin 35 and 7. If present, selection circuit or serial bus control at pins 22-24 may be defective. If no signals were present at pins 9 and 33, go to step 4.
4. Check for 14.318 MHz at pin 18. If not oscillating, check VCXO Bias and filter voltages at pin 17 and 19.

White Stretch

The purpose of the white stretch circuit is to increase luma gain in the low to mid-light regions of the picture on low APL (Average Picture Level) scenes. When the APL is below about 20 IRE, maximum stretch occurs to increase the apparent contrast in the scene. When the APL is above 30 IRE, no stretch occurs. In simpler terms, whenever you have a dark scene with few whites, the white stretch circuit increases the level of the whites to increase the contrast between the white and dark portions of the picture. White and black stretch are sometimes referred to as Dynamic Gamma.

Figure 22 shows a block diagram of how the white stretch circuit operates. The luma input signal is applied to both a linear and a non linear stage. The linear half operates at all times. The non linear section is active with signals above 50 IRE. 100 IRE represents the video voltage which produces maximum white on the screen while 0 IRE represents black.

The output of both stages is applied to the mixer stage which mixes the output of the two stages to produce the white stretched luma output. The amount of mixing is regulated by the mixer control voltage. This voltage is representative of the average picture level (APL). When the APL is low (less than 20 IRE), the control voltage allows the output of the non linear stage to be mixed into the signal. The opposite is true when the APL is above 30 IRE, the linear stage is switched to the output.

The graph at the right of the in figure 22 shows the overall effect of the circuit. The X axis shows the IRE input to the circuit. At 50 IRE in, the white stretch circuit will produce 62 IRE at the output. This represents maximum stretch and occurs only when the APL is less than 20 IRE. When the APL is in the range of 20 to 30 IRE, the amount of amount of stretch lies within the area of the triangle on the graph. Above 30 IRE APL, the output is represented by the straight line which shows no stretch.

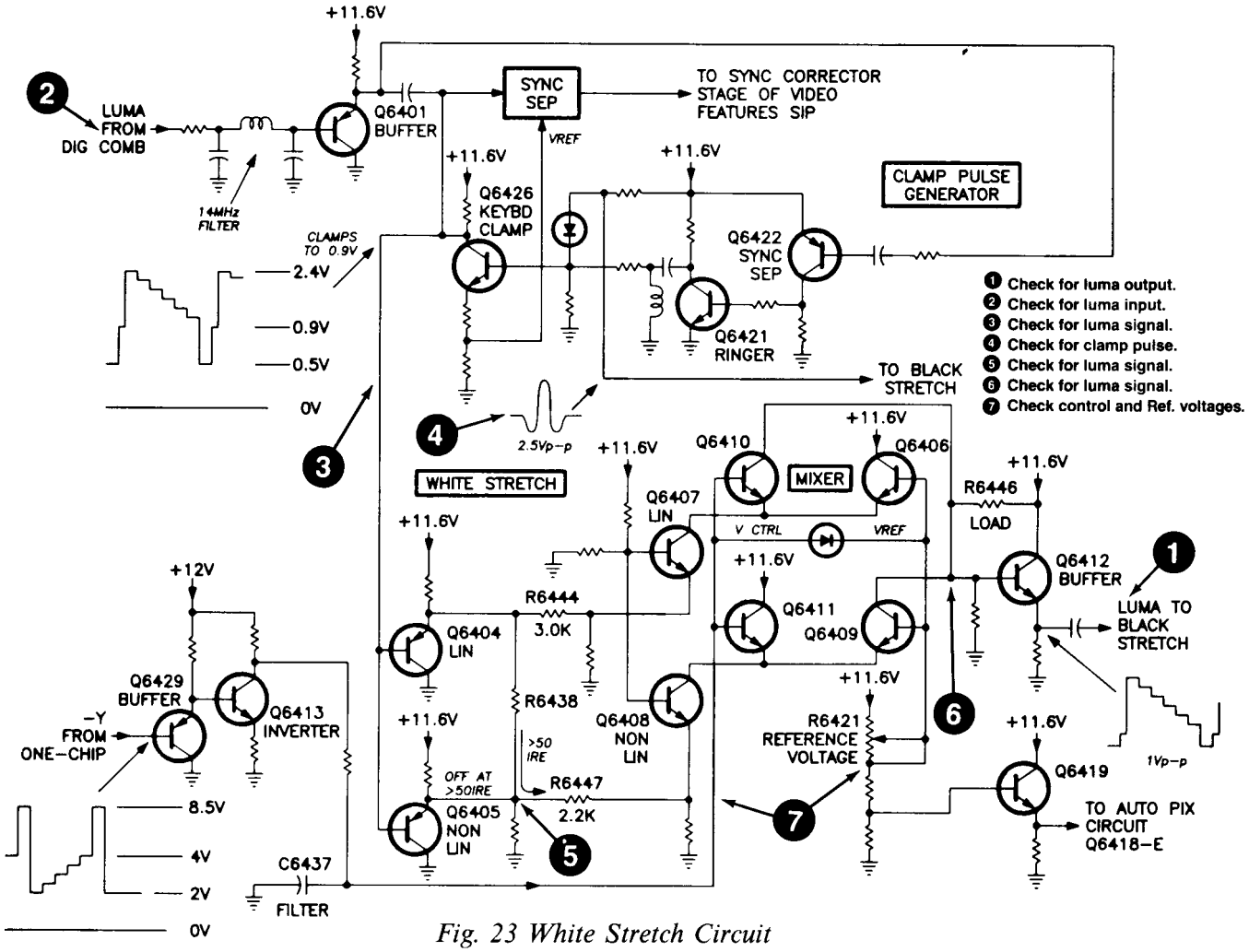


Fig. 23 White Stretch Circuit

The video waveform in figure 22 shows the effect on the video signal after is passes through the white stretch circuit. The 50 IRE portion of the signal is stretched to 62 IRE to produce a brighter image on the screen while the rest of the picture information is unaffected. The result is a higher contrast picture during low APL scenes.

White Stretch Circuit Operation

The luma signal from the digital comb is applied to a 14 MHz LC filter at the base of Q6401 to remove digital noise from the luma signal. Q6401 buffers the signal which then is applied to the white stretch input and to a clamp circuit.

Clamp Pulse Generator

The white stretch circuit requires the input luma signal blanking level be clamped to a known voltage. This is the purpose of the clamp circuit.

The clamp pulse generator develops a clamp pulse during composite blanking. The luma signal from Q6401 is applied to the sync separator Q6422. The composite sync signal from Q6422 is applied to the ringer transistor Q6421. The LC combinations in the collector of Q6421 produces the ringing waveform which is the clamp pulse. The clamp pulse is applied to the base of Q6426 and also to the black stretch circuit.

When the clamp pulse is high during composite blanking, Q6426 turns on to pull the luma signal at its collector to 0.9 VDC. Q6426 turns off when the blanking interval is over. The ringing in the clamp pulse generator quickly turns off Q6426 to prevent clamping during the video portion of the signal. If the clamp pulse is missing, Q6426 never turns on, allowing the DC offset of the luma signal at its collector to rise. This DC offset would not allow the white stretch circuit to operate.

White Stretch Circuit

The clamped luma signal is applied to the bases of Q6404 and Q6405. The signal path from this point on is separated into a linear and a non-linear path.

Signals Above and Below 50 IRE
Both Q6404 and Q6405 are turned on when the luma signal is less than 50 IRE. This produces equal signal voltages at their emitters and across R6438 producing no current flow through it.

When the luma signal rises above 50 IRE, Q6405 turns off due to DC bias on its emitter. However Q6404 stays on to pass the luma signal. Now current flows through R6438 since the Q6405 is turned off. The current through R6438 produces a luma signal at R6447 which is lower in voltage than at R6444.

The luma signals at R6444 and R6447 create a current flow in Q6407 and Q6408 which is proportional to the signal level. Since R6447 is smaller than R6444, the current gain of the Q6408 amp is greater than the current gain of the Q6407 amp. This results is a "stretched" luma signal due to the overall gain of the non-linear channel being greater than the gain of the linear channel for signals above 50 IRE.

Note: No waveforms are visible at the emitters and collectors of Q6407 and Q6408 since the signal is a changing current and not a changing voltage. The voltage waveform may be viewed at the load resistor R6466 at the output of mixer stage.

Linear/Non-Linear Mixing
The linear current through Q6407 is applied to a differential pair consisting of Q6406 and Q6410. The non-linear current through Q6408 is applied to the differential pair of Q6409 and Q6411.

The control voltage at the base of Q6410 and Q6411 is derived from the -Y signal from the one-chip. The -Y signal is applied to the base of Q6429 which buffers the signal and reduces the voltage swing of the blanking pulse to prevent it from affecting the control voltage. The resulting signal is inverted by Q6413 and filtered by C6437 to produce a DC control voltage. When the APL of the -Y signal increases, so does the control voltage. The control voltage generally operates at about 6 to 7 VDC.

The Reference voltage from R6421 is applied to the bases of Q6406 and Q6409. The reference voltage sets the operation point of the white stretch circuit by setting the point at which the linear and non linear circuits are switched into the output. Note that the reference voltage is also buffered by Q6419 to be used as a reference for the Auto-Pix circuit which will be discussed later.

When the control voltage is greater than the reference voltage, Q6410 turns on and Q6406 turns off. The linear current from Q6407 passes through Q6410 and develops a voltage at the load resistor R6446. With the control voltage greater than the reference, Q6411 is also turned on and Q6409 is turned off. The non-linear current from Q6408 passes through Q6411 to the 11.6 volt supply instead of the load resistor R6446.

When the control voltage is less than the reference voltage, the reverse scenario occurs. Q6410 and Q6411 turn off and Q6406 and Q6409 turn on. This allows the linear current to flow into the supply and while the non-linear current produces voltage across the load R6446. R6446 is designed to produce a 1 Vp-p luminance signal at the base of Q6412. Q6412 buffers the signal and provides a low impedance source for the black stretch circuit ahead.

White Stretch Troubleshooting

Symptom: No Video.

1. Check for luma at emitter of Q6412. If present, the problem lies beyond the white stretch circuit. If luma is not present, check for luma at emitter of Q6401. If not present, check circuits prior to Q6401. If luma is present at Q6401, go to step 2.
2. Check DC level of luma signal at collector of clamp Q6426 according to waveform in figure 23. If DC offset is very high, check operation of clamp circuit by checking for clamp pulse at base of Q6426. If not present, check for clamp pulse from ringer Q6421. If luma level at collector of Q6426 is OK, go to step 3.
3. Check for luma signal at base of Q6412. If present, Q6412 may be defective. If luma is not present on the base, check transistor stages between Q6404 and Q6405 up to base of Q6412.

White Stretch Verification
Even though the white stretch circuit is producing a luminance signal at the emitter of Q6412, it is still rather difficult to detect whether white stretching is really occurring by looking at the screen. Use the following procedure to verify operation of the white stretch circuit.

1. Tune the TV to an active channel with many scene changes. Try not to use a test pattern for this procedure. Attach a scope probe to the collector of Q6426. Connect the second probe to the emitter of Q6412.
2. Adjust the vertical gain of the scope to make the signals appear the same amplitude on the scope. Place the scope in the ADD mode and invert one scope channel. Uncalibrate one of the vertical channels to cancel the two signals on the scope to obtain the smallest P-P voltage. If the white stretch circuit is working, you shouldn't be able to obtain 100% cancellation of the two signals and you should see random video information on the scope. If you don't, try another channel. The reason you shouldn't get cancellation is that the output is not a true representation of the input luma signal due to non-linear operation of the white stretch circuit. Since the two signals are not equal, they would not cancel each other totally when inverting and adding them together.

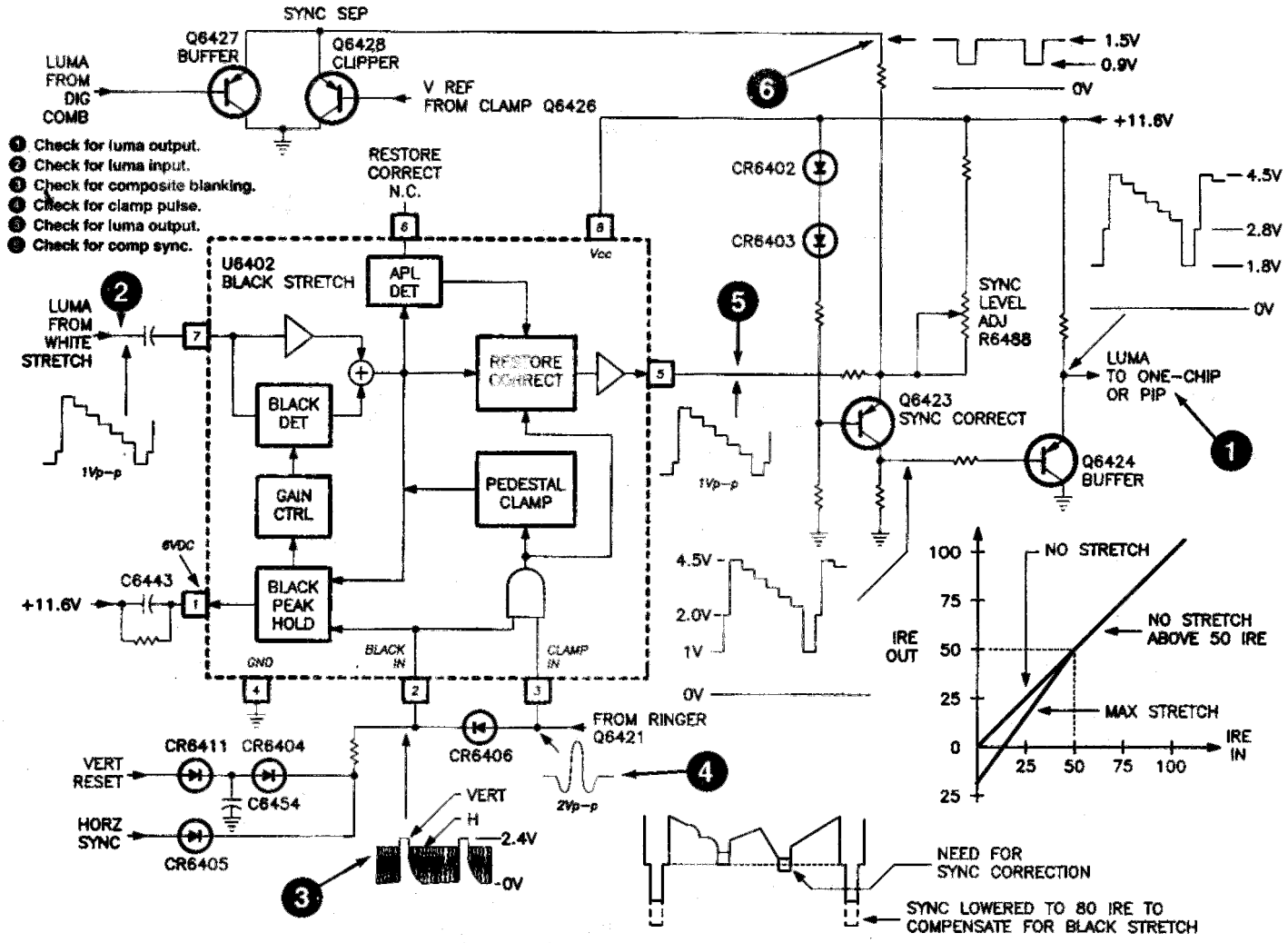


Fig. 24 Black Stretch With Sync Correct

Black Stretch Circuit

The black stretch circuit shown in figure 24 is very similar to the white stretch circuit except the black portion of high APL scenes is stretched instead of the whites. In simpler terms, in bright scenes with few dark areas, the black stretch circuit lowers the level of the dark portions of the scene to increase the contrast between them and the bright portions. The circuit is contained with U6402 unlike the discrete black stretch circuits.

The circuit peak detects the black portions of the luma signal and tries to stretch them to zero IRE. To do this, the circuit changes the luma gain below 50 IRE while having no effect on signals above 50 IRE. Maximum stretch occurs in high APL scenes with few blacks. Note that this is reverse operation of white stretch which operated with low APL. No black stretch occurs in low APL scenes.

Note the graph in figure 24. Signals below 50 IRE are decreased in the output. Note that signals below about 12 IRE are stretched below zero IRE. Since these signals drop below zero IRE, a sync corrector stage must be added to insure these signals are not detected as sync by the sync separator. The straight line signifies no stretch when the APL is low.

Circuit Operation

The luminance signals from the white stretch circuit enters U6402 at pin 7. Inside the IC, the black peaks are detected and applied to the restore correction stage. The APL detect determines how much, if any, black stretch to perform.

The input of the restore correct stage is clamped from a combination of the composite blanking input at pin 2 and the clamp pulse at pin 3. The black stretched luma signal exits the IC at pin 5.

Sync Correction

Notice the waveform at the bottom of figure 24. One of the black stretched signals extends below blanking. This could possibly be interpreted as sync by the sync separator. The sync correction stage prevents this from occurring.

The luma from the digital comb is applied to buffer Q6427. The signal at the emitter of Q6427 determines when clipper Q6428 conducts. The V Ref (about 0.85 VDC) from the emitter of clamp Q6426 is used as a reference to determine where to strip sync from the luma signal. Whenever the signal at the emitter of Q6427 rises above 0.85 VDC, Q6428 conducts to clamp signal to about 1.5 VDC during the non sync portion of the video signal. This produces the composite sync signal at the emitter of Q6428.

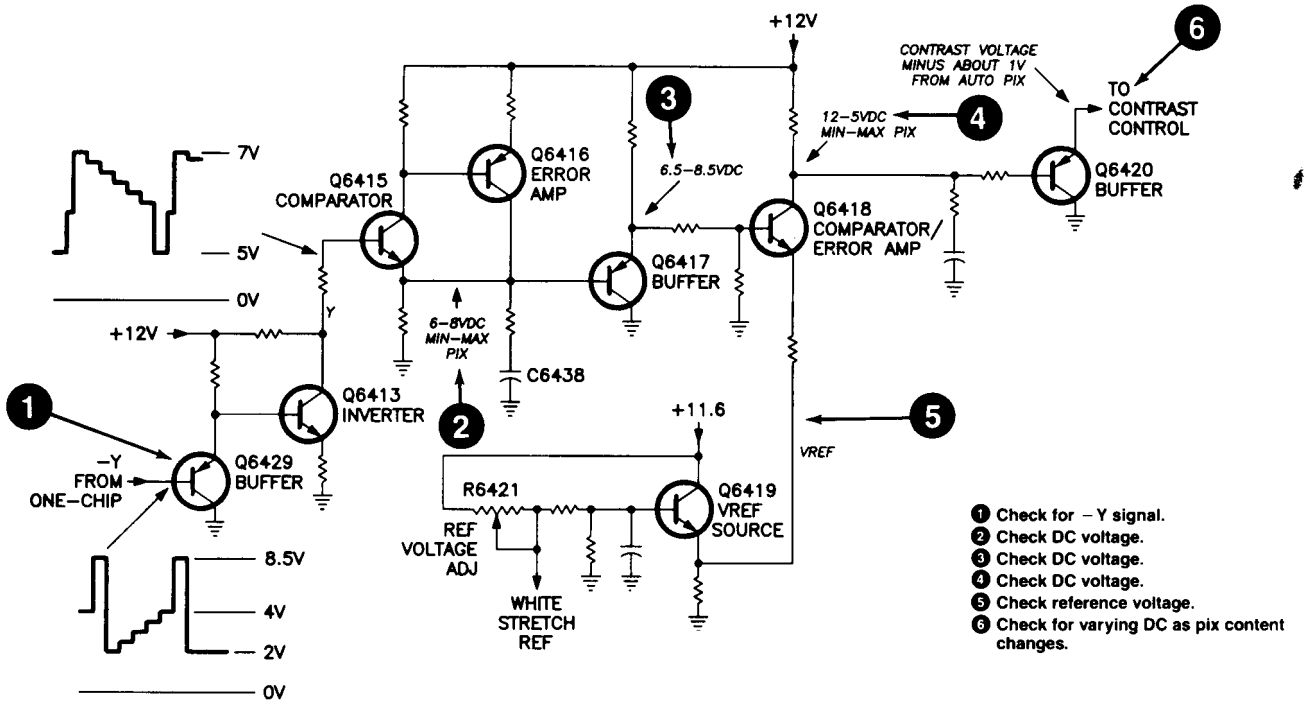


Fig. 25 Auto Pix

The luma from U6402-5 is applied to the emitter of Q6423. When the sync signal from Q6428 goes low, Q6423 turns off to allow the resistor in its collector to set the level of the sync tip. The sync level adjustment R6488 sets the sync level (voltage from sync tip to blanking) by changing the DC level of blanking in the luma signal from pin 5 of U6402.

The signal at the collector of Q6423 is buffered by Q6424 to create the luma waveform shown in figure 54. The luma signal from this point is either applied to the one chip or to the PIP module if so equipped.

Black Stretch Troubleshooting

Symptom: No Video.

1. Check for luma signal at emitter of Q6424. If present, problem lies beyond black stretch circuit. If luma is not present, check for signal at U6402-5. If present, check sync separator and Sync correct circuit. If no luma at pin 5, go to step 2.
2. Check for luma at pin 7. If present, check for composite blanking signal at pin 2 and clamp pulse at pin 3. If OK, suspect U6402.

Symptom: Sync instability in picture.
Check output of sync separator Q6427/Q6428 and check Sync Level Adjust R6488 according to service data.

Black Stretch Verification
Follow the same procedure as White Stretch Verification except place one probe on U6402-7 and the other probe on U6402-5.

Auto Pix (Contrast)

The optional auto pix feature located on the video features sip is used to automatically lower the contrast control voltage to prevent blooming during high contrast scenes.

The input to the auto pix circuit shown in Figure 25 is the -Y signal from the one-chip. The -Y signal is applied to the base of Q6429 which buffers the signal and reduces the voltage swing of the blanking pulse. The resulting signal is inverted by Q6413 to produce the Y signal shown in figure 25.

The comparator Q6416 and error amp Q6416 operate as a peak detector to conduct only during peak portions of the Y signal. The peaks from the Y signal are used to charge C6438 to produce a DC control voltage. The voltage at the emitter of Q6415 varies from about 6 to 8 VDC from minimum pix content to maximum. The positive going peaks of the Y signal can be seen riding the DC voltage at the emitter of Q6415.

The DC control voltage from the emitter of Q6415 is applied to the base of buffer Q6417. The output of the buffer is applied to the base of comparator/error amp Q6418. As long as the voltage a the base of Q6418 is 0.6 VDC above the reference voltage at its emitter, Q6418 conducts to pass the control voltage to contrast control through buffer Q6420. If the picture content drops, so does the control voltage at the base of Q6418. If the voltage at the base of Q6418 drops below the reference voltage at the emitter, Q6418 turns off. When this happens, the contrast control is not affected by the auto pix circuit. Note that the reference voltage is the buffered reference voltage used by the white stretch circuit.

The DC voltage at the collector of Q6418 ranges from about 12 to 5 VDC from minimum pix content to maximum. The capacitance on this line stabilizes the control voltage and prevents oscillations in the contrast control loop. If the contrast control voltage is higher than the voltage at the base of Q6420, Q6420 conducts to pull the contrast control lower to prevent blooming. The contrast control can only be decreased and never increased by the auto pix circuit. The auto pix circuit can decrease the contrast control by about 1 VDC in high contrast scenes.

Auto Pix Troubleshooting

If you have a contrast control problem, disable the auto pix circuit to verify that it is not causing the problem. The auto pix circuit can be disabled by grounding the base of Q6418.

To check the auto pix circuit, verify that the circuit is receiving the -Y signal and confirm the DC voltages shown in figure 25.

CRT DRIVER CIRCUIT

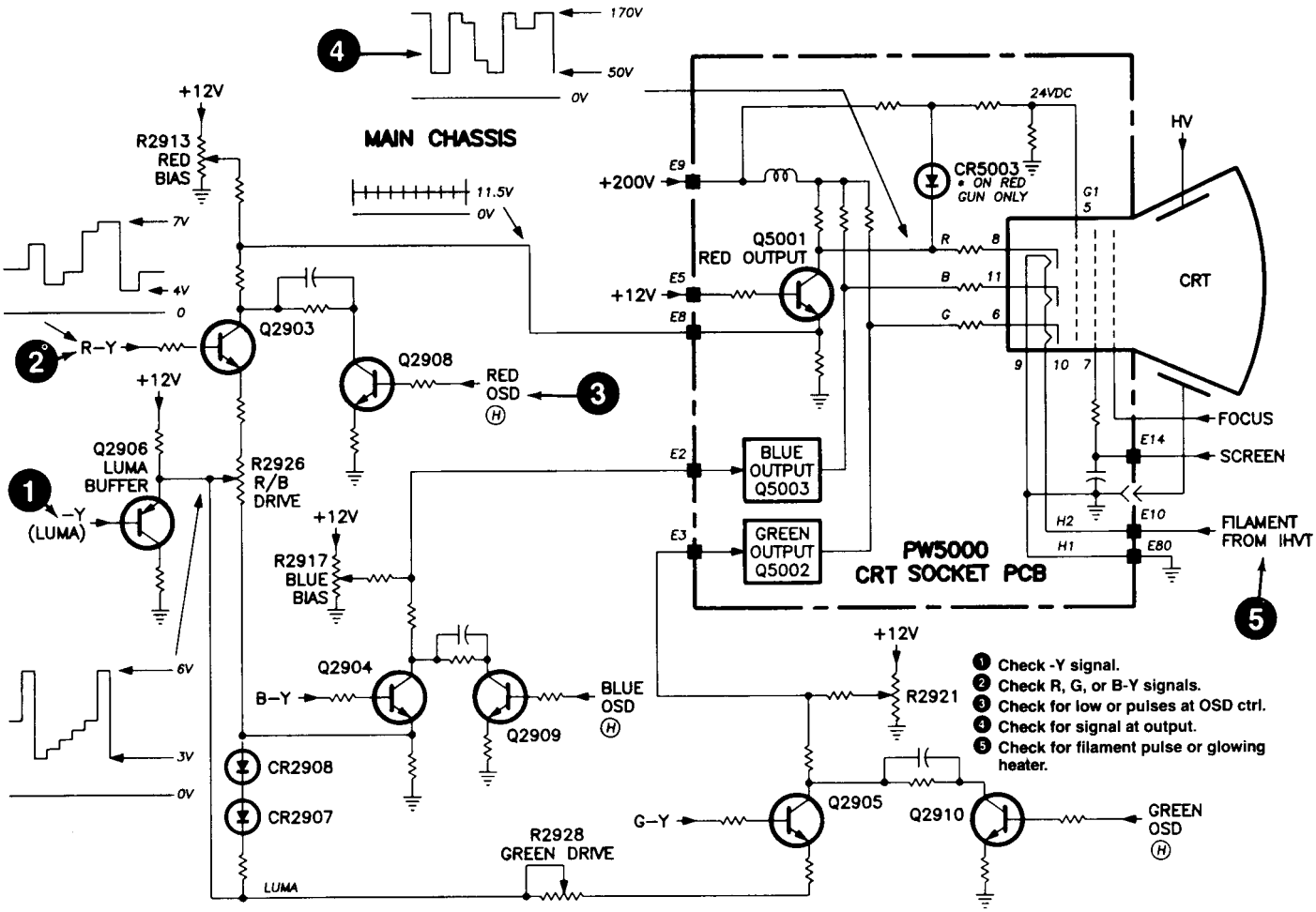


Fig. 26 CRT Driver Circuit (Direct View)

Direct View CRT Board

Since the red, green and blue CRT driver stages are almost identical, only the red stage will be discussed in the circuit description. Any differences will in the stages will be noted.

The R-Y signal for the one-chip is applied to the base of Q2903. The -Y signal form the one-chip is buffered by Q2906 before being mixed with the R-Y information in Q2903. The current through the collector of Q2903 contains both chroma and brightness (luma) information.

The current is applied to the common base amp Q5001 on the CRT board. The current changes in the emitter of Q5001 is converted to a voltage waveform at its collector. The collector is connected to the cathode of the CRT to produce beam current in the red gun. Beam current thought the red cathode increases as the voltage at the cathode is lowered toward ground and decreases as the voltage rises.

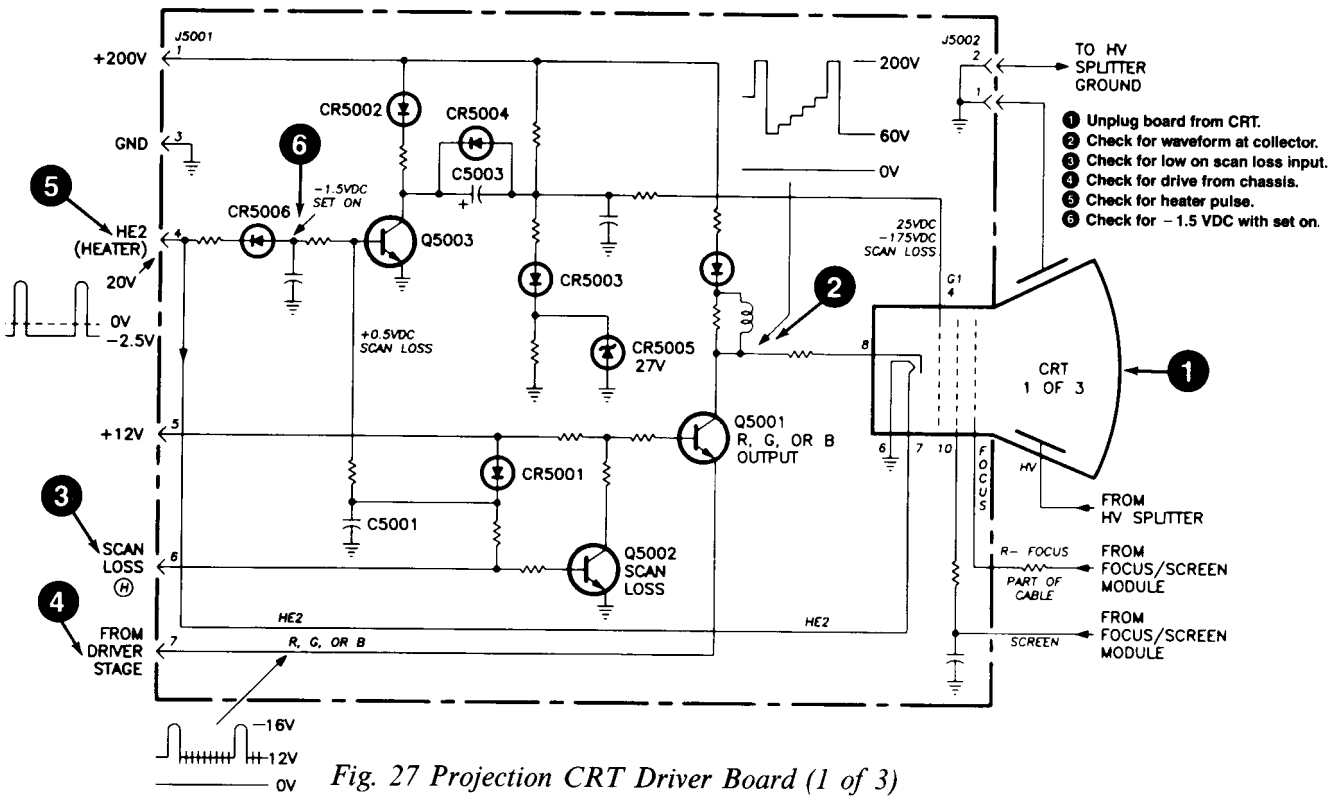


Fig. 27 Projection CRT Driver Board (1 of 3)

The red bias control R2913 adjusts the DC offset of the waveform at the cathode of the CRT while the R/B drive control R2926 varies the peak to peak amplitude of the waveform at the cathode. The R/B drive control affects both the red and blue gun while the green gun has its own drive control R2928.

The blue and green output stages on the CRT board are identical to the red except for CR5003 on the red cathode. This diode is used to prevent grid 1 of the CRT from being more positive than any of the cathodes which would cause grid current.

When the set is first turned on, the beam current limiter circuit is not enabled until the CRT filaments heat and beam current begins to flow. If the scene content contains high IRE whites, the cathodes of the tube may be pulled very close to ground since the contrast control is not yet affected by the beam current limiter. If the cathode drops below the 24 VDC on grid 1, CR5003 conducts to pull the grid voltage within 0.6 VDC of the cathode. Although the grid is positive with respect to the cathode, the 0.6 volts difference is not enough to cause significant grid current.

OSD Drivers

Q2908 on the emitter of Q2903 is used to produce the on-screen display information on the CRT. The base of Q2908 is tied to the red OSD line from the system control micro U3101. To produce a red character on the screen, the red OSD line from the system control micro goes high and turns on Q2908. The current through Q2908 lowers the voltage on the collector of Q5001 to draw current through the red cathode to produce the character on the screen. Note that the blue and green driver stages have their own OSD controls lines from the system control micro.

Notice that the bias controls for the three guns also affects the OSD color temperature where in previous chassis they had no effect.

Projection CRT Driver

Figure 27 shows one of three of the CRT driver boards used in the CTC169 projection models. The circuit is very similar to direct view models except for the scan loss protection circuits.

CRT Driver

The signal drive signal from the main chassis enters the CRT board at pin 7 of J5001. This signal is a current proportional to the signal level and is not a true voltage representation creating the waveform shown in figure 27. The current flows to the common base amp Q5001 which produces the waveform at the collector of Q5001. This waveform was taken with a color bar pattern applied and the color control at minimum. If the color control was not at minimum, the stair step pattern would vary according to the color and tint control settings.

This signal at the collector of Q5001 is applied to the cathode of the CRT. When the cathode is pulled toward 0 volts, beam current increases. A positive voltage at Grid 1 allows beam current to flow. If the voltage goes negative, beam current stops. This action will be used during scan loss to prevent phosphor burning.

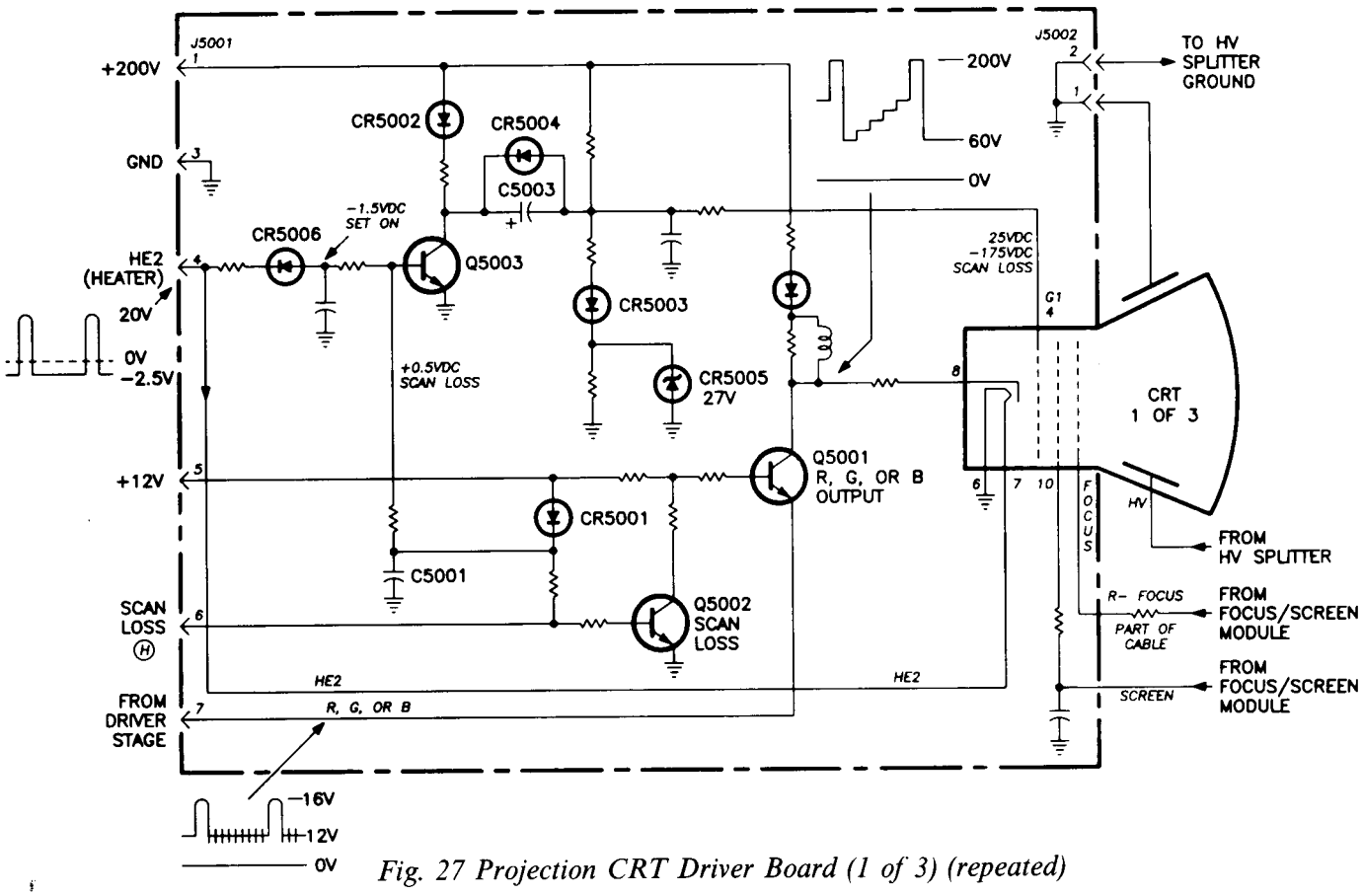


Fig. 27 Projection CRT Driver Board (1 of 3) (repeated)

The screen and focus controls for all three tubes are derived from one Focus/Screen module. The anode of the three CRTs are supplied from a high voltage splitter.

Scan Loss

Scan Present

When the set is operating normally, the scan loss input at pin 6 of J5001 is pulled low by the open collector output of the scan loss detector circuit. This turns off Q5002 allowing the base bias of Q5001 to exist. This allows Q5001 to conduct to produce beam current through the CRT.

The heater pulse at J5001-4 drives the filament of the CRT and also provides -1.5 VDC bias at the anode of CR5006 to turn off Q5003. With Q5003 off, C5003 has 200 volts on its positive terminal and 25 volts (from CR5005) on its negative side. The 25 VDC bias established from CR5005 is also applied to grid 1 of the CRT which allows beam current to flow.

While deflection is running, C5001 charges to 11.5 VDC through CR5001. The charge on C5001 will be used during scan loss to turn on Q5003.

Scan Loss

When scan is lost form either a defect or the set being turned off, the open collector output of the scan loss detect circuit turns off allowing pin 6 of J5001 to float high from the bias at the base of Q5002. This bias turns on Q5002 which turns off Q5001 by removing its base bias. This stops beam current in the CRT.

Since horizontal deflection has stopped, the heater pulse at J5001-4 stops. This removes the -1.5 VDC bias at the base of Q5003. Now the charge on C5001 turns on Q5003. With Q5003 on, the positive terminal of C5003 is grounded. Since it has a 175 VDC charge across it, the grid of the CRT sees -175 VDC. This quickly stops any beam current through the CRT which may not have been stopped by the scan loss Q5002.

Eventually the charges on C5001 and C5003 diminish as well as the other DC supplies to the CRT board. When the set comes back on, the scan loss pin 6 is pulled low allowing Q5001 to operate. The heater pulse turns off Q5003 which returns the grid bias to 25 VDC.

CRT Driver Troubleshooting

When troubleshooting the CRT driver board, unplug it from the CRT to prevent accidental phosphor burns. With the tube disconnected, the waveform at the collector of Q5001 will dip down to about 20 VDC instead of the 60 VDC as shown in figure 27.

Scan loss verification

With set running, check for 25 VDC at the grid 1 (anode of CR5004) of the CRT and for a low at pin 6 of J5001. Check for -1.5 VDC at anode of CR5006.

When the set turns off, check for -175 VDC at grid 1 of the CRT. This voltage will slowly discharge to zero volts. Also check for a high at J5001 pin 6 when the set first turns off. This voltage will slowly discharge when the set is off since it is derived from the + 12 VDC run supply.

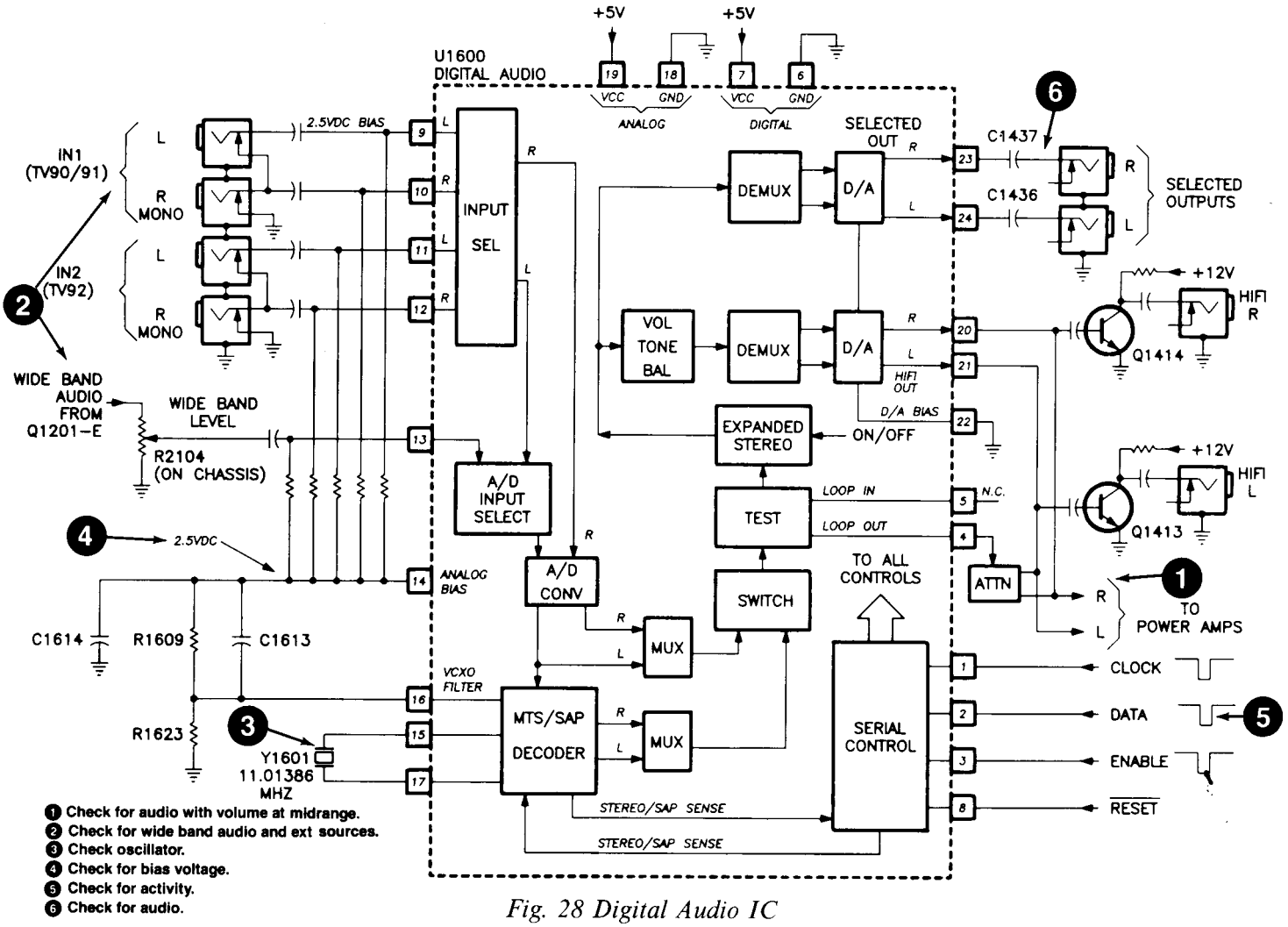


Fig. 28 Digital Audio IC

Digital Audio IC U1600 Overview

All audio functions except power amplification in the CTC168/169 are performed by the digital audio IC U1600. It performs audio source selection, MTS/SAP decoding and selection, expanded stereo operation, volume, tone and balance. All audio enters the IC in analog form, is converted to digital for processing, and reconverted to analog prior to power amplification. Looking at figure 28, you'll notice that there is only one alignment, Wide Band Audio Level. The IC is controlled by a 3 wire serial communications bus from the system control IC.

Input Selection

U1600 selects one of three audio sources: The wide band audio from the internal tuner and two external stereo audio inputs from the back panel. The input selection is controlled by the serial clock, data, and enable lines from the system control micro. There are no individual control lines for audio selection from the micro as in the video selection stages of this chassis.

A/D Conversion

The audio signals are all biased to 2.5 VDC before entering the IC at pins 9 through 13. The bias voltage is provided by pin 14 of U1600. The input 1 audio source is heard by selection TV CH 91 or CH 90 (S-VIDEO). Input 2 audio is heard by selection TV CH 92. The right output of the input select stage is applied directly to an analog to digital converter. The left channel goes to the A/D input select stage which chooses between the left external channel or the wide band audio signal from the tuner. The output of the A/D input select stage is applied to the A/D converter.

MTS/SAP Decoding

When the TV tuner is selected, the digitized wide band audio signal is decoded by the MTS/SAP decoder. The 11.01386 MHz oscillator runs at 700 times the stereo pilot signal and is phase locked to it during stereo reception. The VCXO filter at pin 16 affects the phase locking operation. The VCXO pin 16 is biased to 2.5 VDC from the analog bias pin 14. C1614 is the filter cap for the analog bias voltage. If this cap is defective, you will hear loud motorboating from the speakers. C1613 is a filter cap for the VCXO pin 16. If it is defective, the VCO will not lock the pilot signal and give you random stereo reception accompanied by static in the audio.

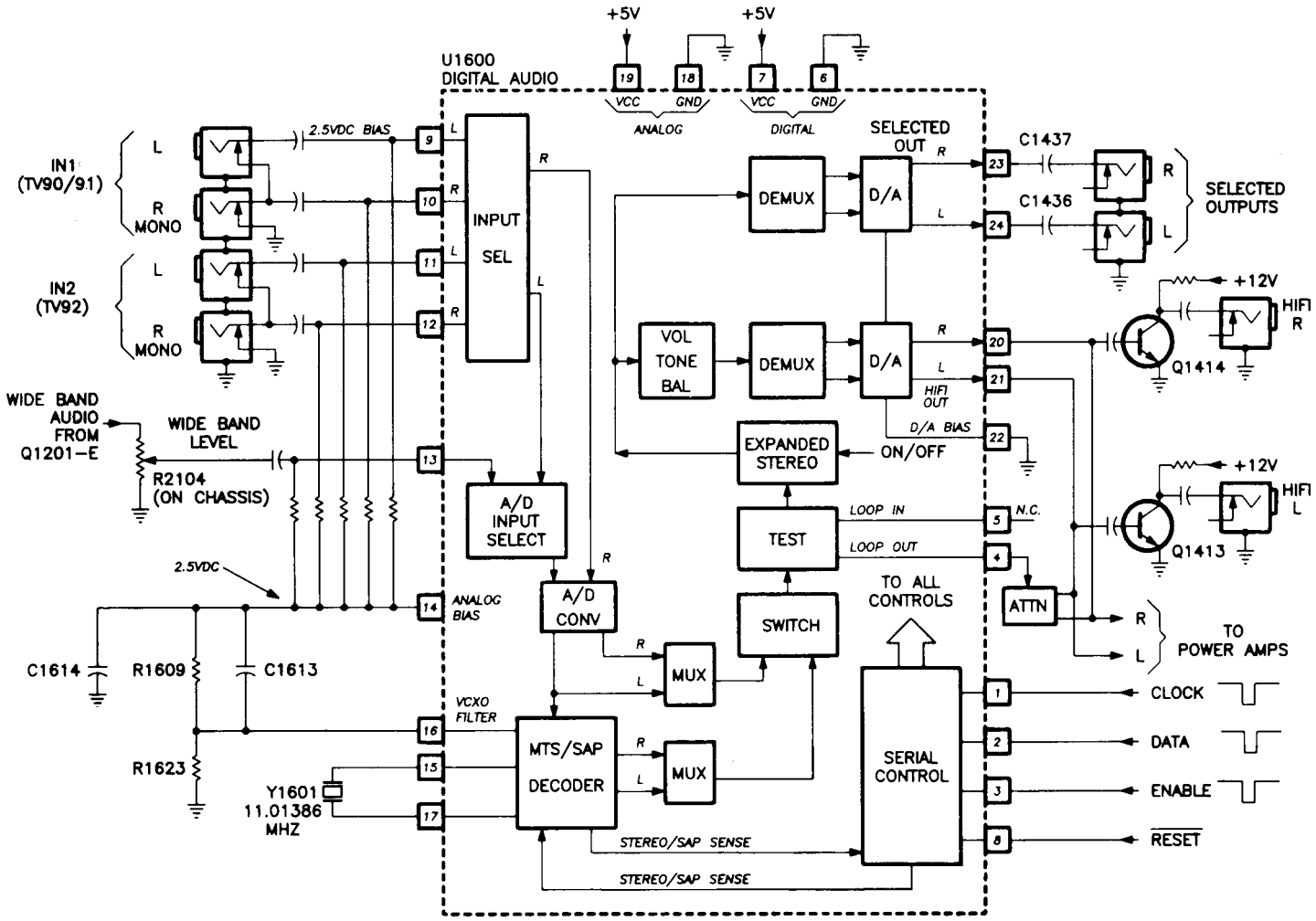


Fig. 28 Digital Audio IC (repeated)

The free run frequency of the oscillator at pin 15 should be 11,014,000 Hz ± 500 Hz with a mono station tuned and mono mode selected in the audio menu. The VCXO cannot lock to the pilot signal if the free run frequency is too far off.

The system control micro checks for the availability of stereo and sap about four times per second through the serial control bus. If stereo or sap is present and is selected in the audio menu, U1600 is commanded by to the system control micro to select stereo or sap.

The right and left outputs of the MTS/SAP decoder are multiplexed together and applied to a switch which selects between the tuner audio or the external audio sources. The output of the switch passes through a test stage. The test stage is for manufacturing use and does not contain any test routines for the servicer. The loop out of the test stage will be used in some chassis to attenuate the audio signal at low volume levels to reduce the noise content of the audio signal. This circuit will be used on a break-in basis and may not be used in early production chassis. The attenuator will be covered in the next section of this manual.

The digital audio signal from the test stage is processed by the expanded stereo stage to increase the stereo separation effect. Expanded stereo can be turned on and off from the audio menu.

Volume, Tone, and Balance and HiFi Outputs

The output of the expanded stereo stage follows two paths. One path is through the volume, tone and balance stage. All three settings are controlled internally from the serial communications bus instead of individual voltage controlled inputs as in previous chassis. Muting is also performed at this stage during channel change and when the customer presses the mute button on the remote control.

After the volume, tone, and balance control, the audio signal is demultiplexed to produce individual right and left channel digital information. The digital to analog converter stage then produces right and left analog signals at pins 20 and 21. These signals are buffered by Q1413 and Q1414 and passed to the HiFi output jacks on the back of the set. Remember that the right and left audio from the selected output jack is volume, tone, and balance controlled. This allows remote operations of these settings when connected to an external power amp.

The right and left outputs at pins 20 and 21 are also applied to the internal power amplifier in the TV. The power amp will be covered in the next section of this manual.

Selected Audio Outputs
The other path for the output of the expanded stereo stage is to a demultiplexer stage and a digital to analog converter. The right and left outputs of this D/A are at pins 23 and 24 and are capacitively coupled to the selected output jacks on the back of the set. The audio source for these jacks are the same as for the HiFi output jacks except they are not affected by the volume, tone, and balance controls.

Clock, Data, Enable, and Reset
As mentioned in an earlier paragraph, all commands are delivered to U1600 through the serial communications bus. Refer to the system control section of this manual for serial bus operation and troubleshooting.

Digital Audio IC Troubleshooting

Symptom: No audio.
1. Make sure volume is not at minimum and speakers are turned on in audio menu and connect an audio source to one of the external audio input jacks on the back of the set. If audio can be heard, the problem must lie in the wide band audio from the tuner or in the MTS/SAP Decoder section. If no audio can be heard from either internal or external, go to step 2.
2. Check for audio at pins 20 and 21 of U1600. If present, the problem may just be in the power amp stage. If audio is not present at pins 20 and 21 but is present at pins 23 and 24, the problem must lie in the volume control section of U1600 or in the serial communications bus.

Symptom: OSD Stereo indicator never shows stereo on known stereo station.
1. Select mono mode in audio menu.
2. Connect 10x low capacity probe to pin 15 of U1600 and measure frequency with frequency counter. Should read 11,014,000 Hz ± 500 Hz.
3. Check for defective C1613 or C1614.
4. Check for 2.5 VDC at U1600-14.
5. Check wide band audio level and bandwidth.

Symptom: Poor stereo separation.
1. Adjust wide band audio level according to service data.

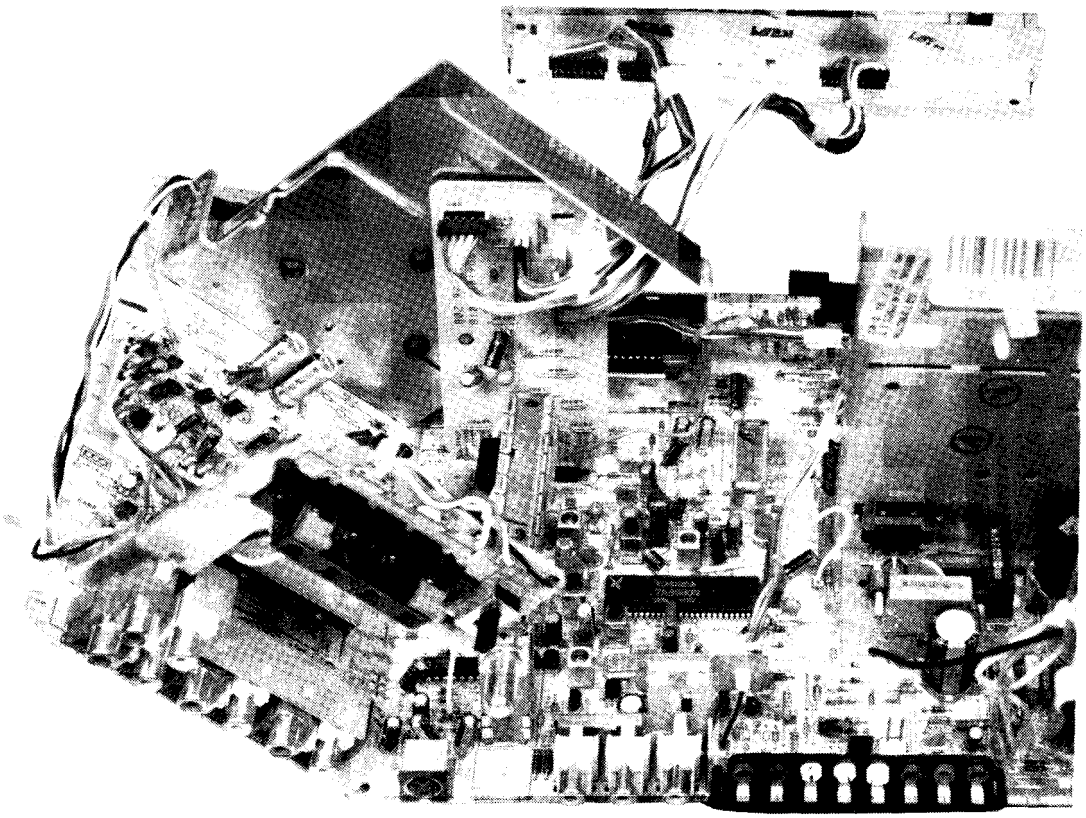


Fig. 29 Audio Service Position

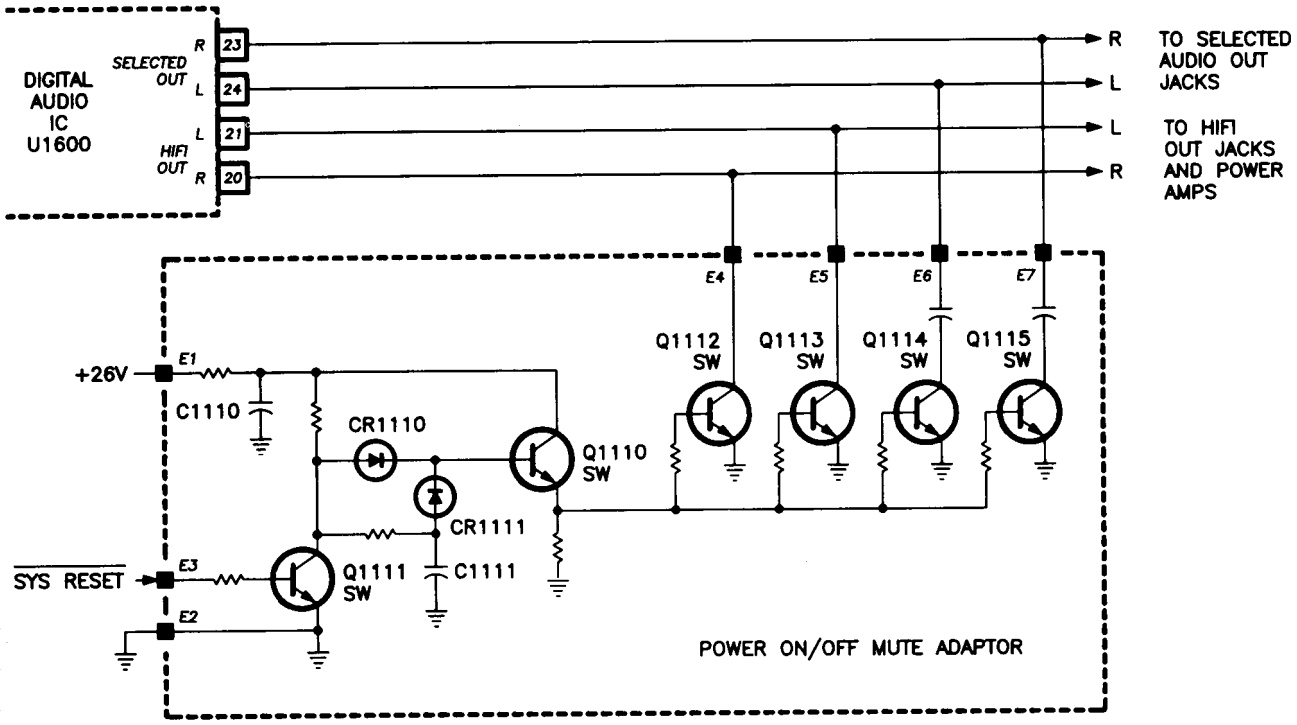


Fig. 30 Power On/Off Audio Mute

Power ON/OFF Audio Mute Circuit

The speaker on/off control prevents pops in the internal speakers of the set during power on/off but has no effect on the Selected and HiFi audio out jacks which may be connected to an external audio amplifier. Figure 30 shows the circuit used to prevent these pops from occurring. The circuit may be mounted on an adaptor board or may be populated on the audio sip board. The circuit operates the same regardless of where it is located.

Set Off

When the set is turned off, the 26 volt supply is available to charge C1111. The system reset line is low and keeps Q1111 off. The 26 volt supply also biases Q1110 on through CR1110. With Q1110 conducting, its emitter voltage turns on Q1112 through Q1115. These transistors mute the right and left audio signals from the Selected and HiFi outputs of U1600. With the set off, no audio is present to mute although any power on transitions will be removed from the output jacks when the set turns on.

Set Off to On Transition

When the set is first turned on, the system reset line stays low for about one second and then goes high until the set is turned off. After the system reset line goes high, Q1111 turns on to ground the anode of CR1110. This removes the 26 volt supply bias from the base of Q1110. However Q1110 stays on due to the charge on C1111. Eventually C1110 discharges and Q1110 turns off to remove the voltage from its emitter. With the emitter voltage gone, Q1112 through Q1115 turn off to unmute the audio lines.

Set On to Off Transition

When the set enters the off state, the system reset line goes low. This turns off Q1111 and applies base bias from the 26 volt supply to Q1110. Q1110 turns on to supply voltage to its emitter to turn on all the mute transistors Q1112 through Q1115.

Troubleshooting Tip

If you encounter a no audio symptom, check Q1110 in the power on/off mute circuit. There should be no voltage at the emitter of Q1110 after the set is on for at least 5 seconds. If there is voltage at the emitter, Q1112 through Q1115 will be turned on to mute the audio.

Audio Power Amplifier - 1 and 5 Watt

Power Amplifier

The right and left volume, tone, and balance controlled audio outputs from the digital audio IC U1600 are capacitively coupled to the power amp U1900. The power amps for both right and left channels are contained within U1900. U1900 can be operated as a 1 watt or 5 watt amplifier. The capacity of the output coupling caps is increased in the 5 watt system. The speaker impedance in the 5 Watt system is lowered to 8 ohms instead of 32 ohms used in the 1 watt system. Both systems run U1900 at 24 VDC at pin 9.

Note: When the TV is turned off, about 22.5 VDC is still present from the 24 Volt supply at pin 9 of U1900 since power is supplied from chopper transformer which runs when the set is turned off. Remove AC power from the set before servicing the audio power amp.

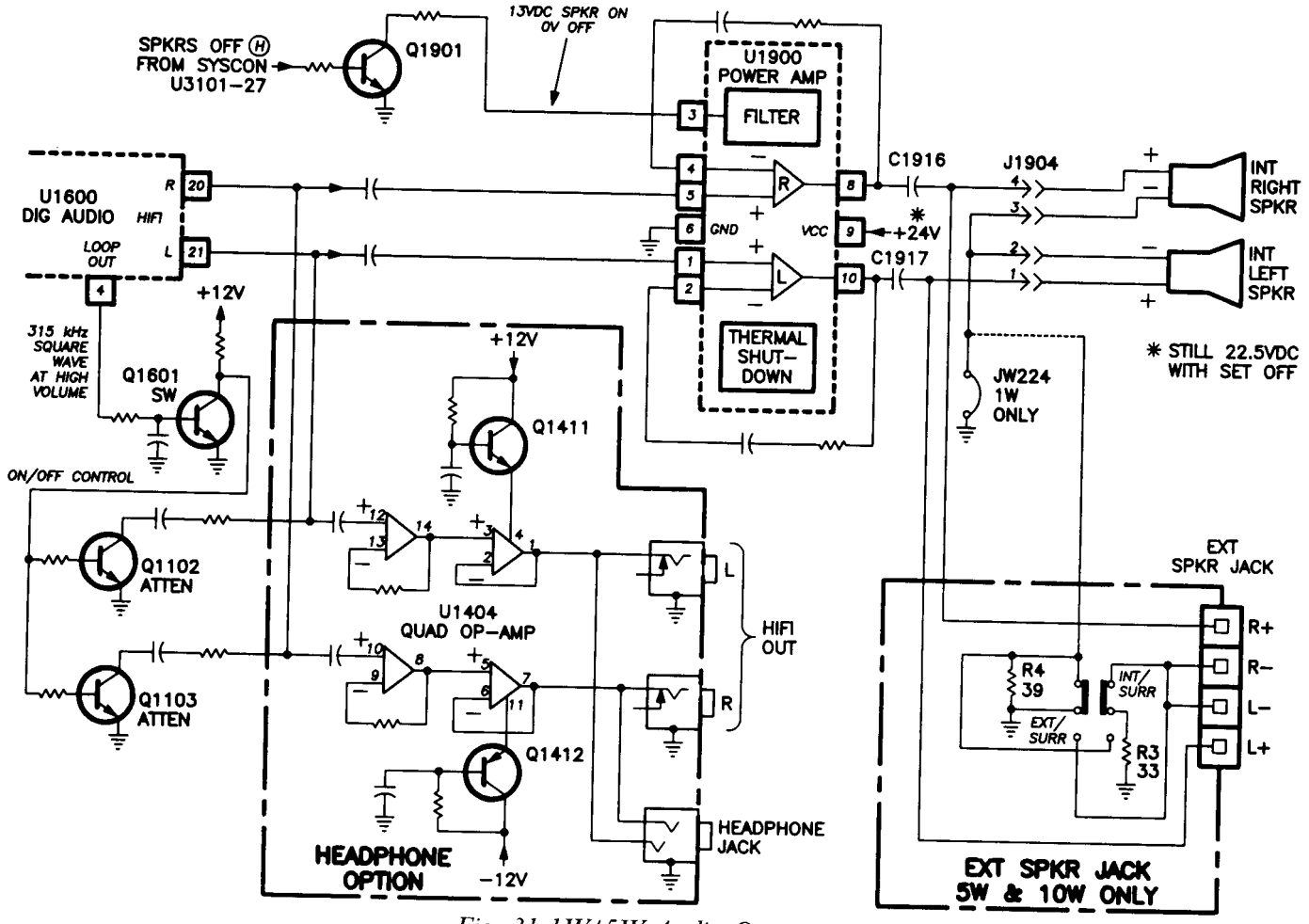


Fig. 31 1W/5W Audio Output

A larger heat sink on U1900 is required to dissipate the additional power of the 5 watt amp. U1900 contains an internal thermal shutdown circuit to protect the IC under extreme loads. If the audio output fails to operate, turn the set off and allow U1900 to cool.

Low Volume Attenuator

During low volume levels, the attenuator circuit tied to the right and left outputs of U1600 decreases the level of the audio signal to decrease noise in the audio output. As mentioned in the previous section, early production sets may not have the software and hardware installed to activate the attenuator.

During mid to high volume settings, the system control micro instructs U1600 to produce a 315 kHz square wave at its loop output pin 4. This signal is filtered by the R/C circuit at the base of Q1601 to produce a DC voltage to turn on Q1601. This produces a low at the collector of Q1601 which turns off attenuators Q1102 and Q1103. With Q1102 and Q1103 off, the right and left audio signals are not attenuated.

At low volume levels, the square wave from U1600-4 is turned off by the system control micro. The bias at the base of Q1601 diminishes turning it off. This produces 12 VDC at the collector of Q1601 which turns on Q1102 and Q1103. The right and left audio signals are attenuated by the R/C path to ground through Q1102 and Q1103.

Speaker On/Off Control

The speakers, both internal and external, may be turned off from the audio menu. The system control micro U3101 drives the SPKRS OFF line at pin 27 high to turn the speakers off. The Hi turns Q1901 on which pulls the 13 volt bias at U1900-3 to zero volts. This in turn disables the power amp.

When you turn the set on, the system control keeps the speakers off until about three seconds after the set is turned on. This prevents pops in the speakers as the audio circuits power up. When you turn the set off, the speakers are tuned off before the set is shut down to prevent pops as the audio circuits turn off.

When troubleshooting loss of audio symptoms, be sure to check for 13 VDC at pin 3 of U1900 before assuming the IC is bad.

External Speaker Jack and Surround Switch

The output of the power amp is applied to the positive side of the internal speakers and to the positive terminals of the external speaker jacks. The external speaker jack is only available in 5 and 10 watt systems.

The INT/SURR switch selects the ground path for both the internal and external speakers. In the INT/SURR position, the negative side of the internal speakers are tied directly to ground while the external speakers are grounded through the 33 ohm R3. This makes the inter-

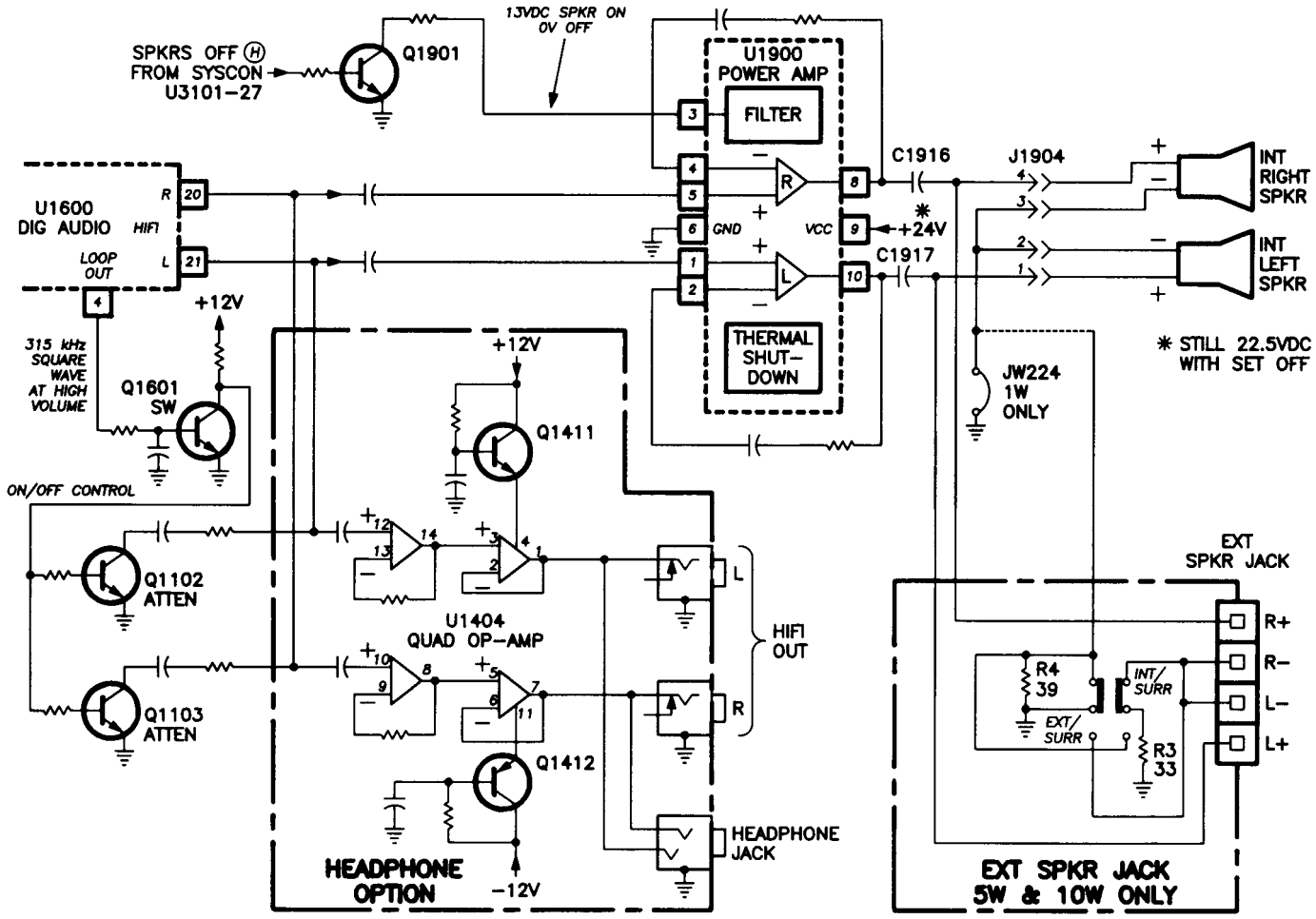


Fig. 31 1W/5W Audio Output (repeated)

nal speakers louder than the external speakers making the external speakers act as the surround speakers.

In the EXT/SURR position, the external speakers are tied directly to ground. The internal speakers are tied to ground through the parallel combination of R3 and R4, about 18 ohms. Now the external speakers are louder than than the internal speakers which act as the surround speakers.

Headphone Option
Some models are equipped with a headphone jack as shown in figure 31. The volume, tone, and balance controlled outputs of U1600 are buffered by the quad op amp U1404 to provide the drive for the headphones. The HiFi outputs are also taken from this buffer circuit instead of the single transistor buffer shown in figure 28. This circuit allows the customer to turn off the internal and external speakers and use remote volume control to adjust the headphone volume.

1W/5W Audio Power Amp Troubleshooting

Symptom: No audio from speakers.
1. Check for audio at U1600 pins 20 and 21. If present, go to step 2. If not present, troubleshoot U1600.
2. Check for signal at pins 5 and 1 of U1900. If present, check for 24 VDC at pin 9. If heat sink is extremely hot, turn off set and let cool. Turn set on to see if audio returns. If not, to to step 3.
3. Check for about 13 VDC at U1900-3. If zero volts, check for proper operation of SPKRS OFF control line at system control U3101-27 or defective Q1901. If OK, go to step 4.
4. Check output coupling caps and speaker continuity.

10 Watt Audio Power Amp with Fault Detect

Figure 32 shows the 10 watt/channel audio output stage used in all CTC169 projection sets. The power amps consist of separate ICs U1901 and U1902. Each IC is powered by a +17 and -17 VDC supply as opposed to +24 for the 1 and 5 watt amps. Also note that the outputs of the power amps are direct coupled (no capacitors) to the speakers.

The speaker On/Off control is tied to pin 4 of each power amps to disable them to turn the speakers off. The control operates just as it did in the 1 and 5 watt amps except for some DC voltage differences. With the speakers on, about 6 VDC is present at pin 4 of the power amp ICs. The voltage at pin 4 drops to about 1.2 VDC with the speakers off.

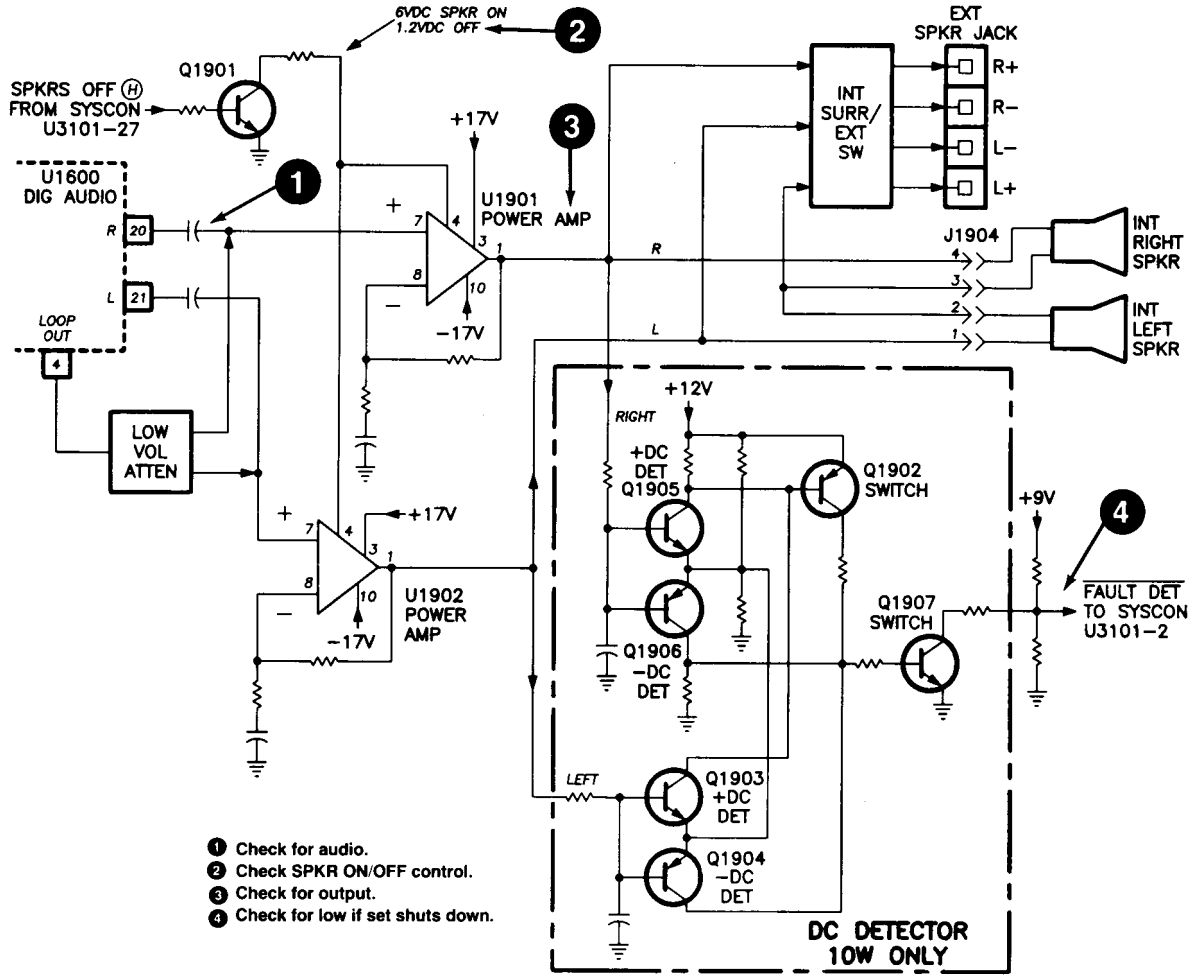


Fig. 32 10W Audio Output With Fault Detect

The internal/external speaker switching is also identical to the 5 watt audio amp as described in the previous section.

The low volume attenuator operates as described in the 1 and 5 watt audio section.

Fault Detect Circuit

Since the 10 watt audio system is direct coupled to the speakers, a DC fault detector is needed to prevent high DC voltages at the amplifier outputs from destroying the power amps and speakers. The fault detector is designed to turn the TV off when a high positive or negative DC voltage is detected on the audio output lines.

Whenever the DC level reaches approximately 2 VDC, Q1905 turns on and pulls the base of Q1902 low. This turns Q1902 on which turns on Q1907. The collector of Q1907 pulls the Fault Detect line low to inform the system control micro to turn the set off. After about 2 seconds, system control turns the set back on. If the fault still occurs, it will turn the set back off. If this occurs 3 times in one minute, system control keeps the set off.

If the DC voltage at the audio output reaches approximately -2 VDC, Q1906 to turn on Q1907. When Q1907 turns on, its collector pulls the Fault Detect line low to initiate the shutdown sequence.

Q1903 and Q1904 perform the same voltage detection for the left audio channel. A defect in either or both channels will cause the fault detect line to go low.

Fault Detector Troubleshooting

1. If you suspect the set is shutting down due to the fault detector, place the Int/Surr switch to the Ext/Surr position and disconnect any external speakers. Ground the base of Q1907 and turn the set back on. If it still shuts down, the shutdown must be caused by the loss of the 9 volt run supply. If the shutdown stops, immediately turn the set off and check the audio output stage for shorts or a defective components. Before returning the set to the customer, be sure to place the Int/Surr switch to the internal position. Check the voltage on the collector of Q1907. If it goes low when the set is on, the fault detector is causing the shutdown. If it never goes low, your problem lies elsewhere. Go to step 2.
2. If the fault detector is causing the shutdown, check the right and left power amp outputs for high DC offsets that could the fault detector to trip. If the outputs appear OK, the problem may be in the fault detector itself.

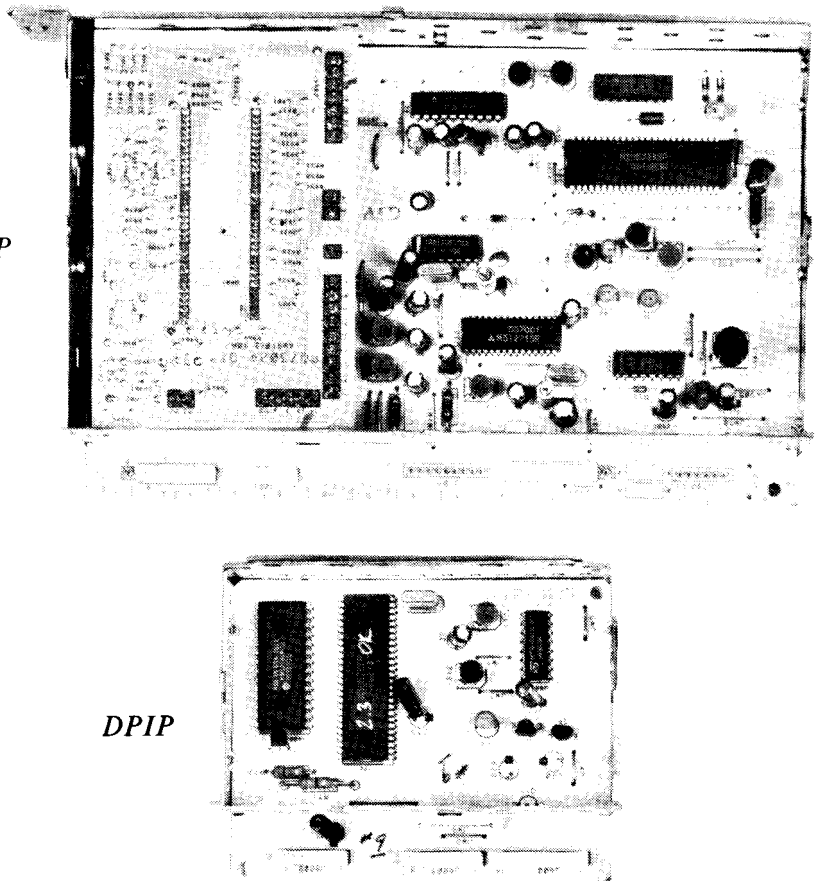


Fig. 33 SPIP & DPIP Modules

There are three pix-in-pix modules used in the CTC168/169 chassis series, DPIP, defeatured SPIP, and full featured SPIP. The following sections of this manual will use the following abbreviations for the three modules:

1. DPIP = DPIP
2. Defeatured SPIP = D-SPIP
3. Full Featured SPIP = FF-SPIP

The DPIP module produces an insert pix (small pix) which can be frozen, moved to one of four positions, and swapped with the big pix. The D-SPIP module performs the identical functions of the DPIP module and is used as a DPIP substitute in early production sets. The FF-SPIP module contains the features of DPIP plus features similar to the ones used in CPIP in the CTC140 chassis. The only electrical differences between the D-SPIP and FF-SPIP module are the signal source for the big and small pix clamp stage and the software in the control micro U8901 in the module. In the future, the FF-SPIP module *may* be a direct substitute for the DPIP module which will elilminate the need for a separate D-SPIP module. The following section covers the features of all modules in more detail.

Note: Due to parts availability, some DPIP sets may contain the D-SPIP module to perform the DPIP functions. Except where noted, the circuit descriptions used for the full featured SPIP module will also apply to the defeatured SPIP module when used as a DPIP substitute. Since some full featured SPIP features will not be used in the defeatured SPIP module, various control lines in the module will not be utilized as described in the full featured SPIP application. These exceptions will be noted in the circuit description.

Note: Just because the PIP circuits are contained within a module does not necessarily mean they are warranty replaceable. Every attempt should be made to troubleshoot to the component level instead of replacing the module.

DPIP and SPIP Operation Guide

Both DPIP and SPIP modules allow you to view an external video source in the small pix while watching the TV tuner in the big pix area or vice versa. The FF-SPIP module also allows the user to freeze and zoom the big picture in addition to the multi-channel feature.

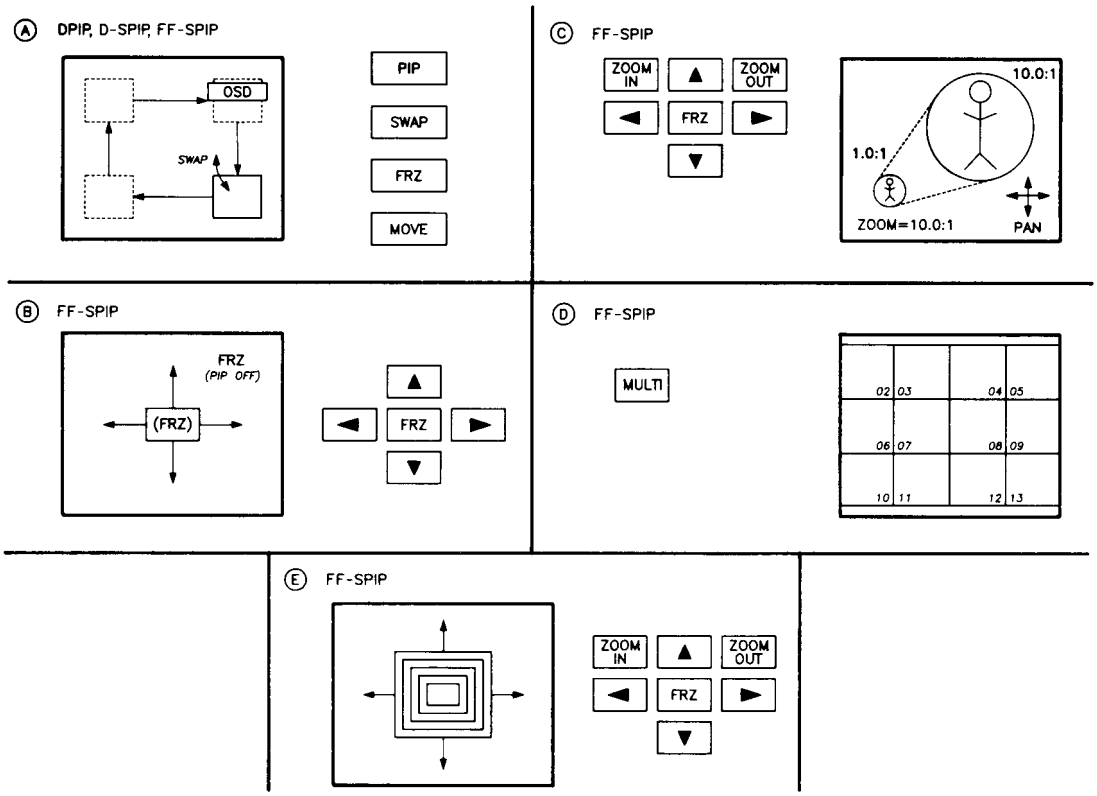


Fig. 34 DPIP/SPIP Operation Guide

The following section gives a brief overview of how some of the most frequently used DPIP and SPIP features operate. Figure 34 shows the required keypresses to operate the features. Refer to the owners manual for a more complete and detailed explanation.

PIP, Swap, Freeze, and Move - Diagram A

The buttons shown in diagram A are all the functions performed by the DPIP and D-SPIP modules. These functions are also performed by the FF-SPIP module in addition to the features shown in diagrams B through E.

PIP

Pressing the *PIP* button activates the Pix-in-Pix feature. The small pix will appear on the screen and contain the same video information as that of the big pix. The audio you hear will always belong to the big pix.

Since the chassis does not contain two tuners, an external video source must be connected to the receiver to obtain a small pix source that is different from the big pix. To select a new source for the small pix, select TV 90, 91, or 92. For 90 and 91, Aux 1 video appears in the small pix; for 92, Aux 2 video. Two separate external inputs cannot be displayed on the screen at the same time.

Pressing the TV button will display the word "PIP" followed by the channel number of the insert video. After a few seconds, the display will change to the big pix channel number.

Press the *PIP* button again to turn off the Pix-in-Pix feature.

Swap

Pressing the *SWAP* button exchanges the big and small pictures. The video previously in the big pix will enter the small pix while the video previously in the small pix becomes the video in the big pix. The audio also swaps to keep the big pix paired with its corresponding audio source. Pressing *SWAP* a second time returns the big and small pix to their original sources.

Freeze

Pressing the *FRZ* button with Pix-in-Pix turned on freezes (still picture) the small pix video. Pressing the *FRZ* button again unfreezes the small pix.

Move

Each press of the *MOVE* button steps the small pix in a clockwise direction to one of the four positions shown in the diagram.

Variable Move and Freeze (FF-SPIP only) - Diagram B

Variable Move

The small pix can be moved to any position on the screen by using the four arrow buttons shown in Diagram B. Pressing and holding one of the four arrow buttons scrolls the small pix in the direction of the arrow. The small pix continues to move until the arrow key is released or the edge of the screen is reached.

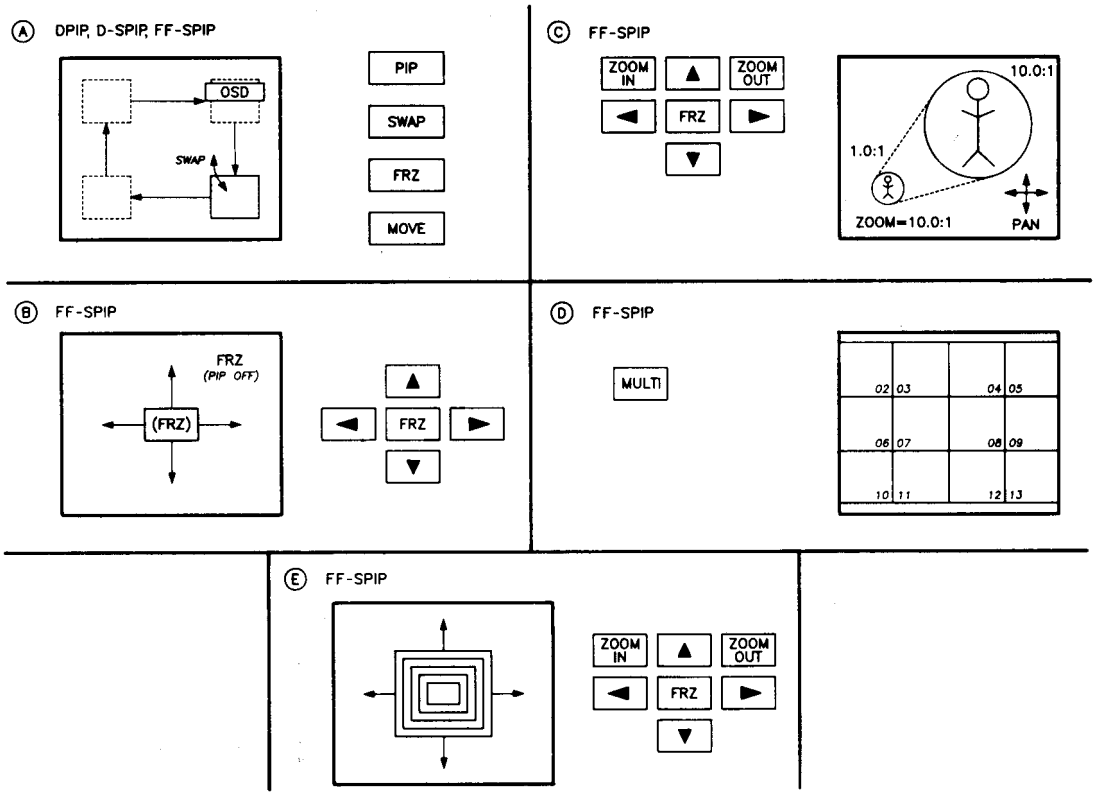


Fig. 34 DPIP/SPIP Operation Guide (repeated)

Zoom In/Out (PIP ON - FF-SPIP only) - Diagram E

Zoom In
With Pix-in-Pix enabled, pressing the *ZOOM IN* button increases the size of the small pix to one of five preset sizes. Each press of the *ZOOM IN* key advances the size to the next larger increment until the largest size is reached. The arrow keys still move the small pix as described earlier. The *FRZ* key freezes the small pix regardless of its size.

Zoom Out
With Pix-in-Pix enabled, pressing the *ZOOM OUT* button decreases the size of the small pix to one of five preset sizes. Each press of the *ZOOM OUT* key decreases the size to the next smaller increment until the smallest size is reached.

Zoom In/Out and Pan (PIP OFF - FF-SPIP only) - Diagram C

Zoom In
With Pix-in-Pix turned off, pressing the *ZOOM IN* button increases the size or zooms in on the content of the big pix. The zoom ratio begins at 1:1 and increases to 10:1. The zoomed picture can be frozen by pressing the *FRZ* button just as during non-zoom operation.

Zoom Out
Pressing the *ZOOM OUT* button decreases the zoom effect and eventually brings the picture back to the 1:1 (normal viewing) ratio.

Panning
While in the zoom mode, you may search or pan through the picture content by pressing one of the four arrow keys. Then the screen image will move across different areas of the picture.

Multi Channel (FF-SPIP only) - Diagram D

Pressing the *MULTI* button activates the multi channel mode which cycles through the scan list and displays a frozen pix from each channel on the screen. One active and eleven frozen channels can be displayed on the screen at once. The feature will continue to cycle through the scan list until the *MULTI* button is pressed again. The multi channel display can also be frozen and zoomed.

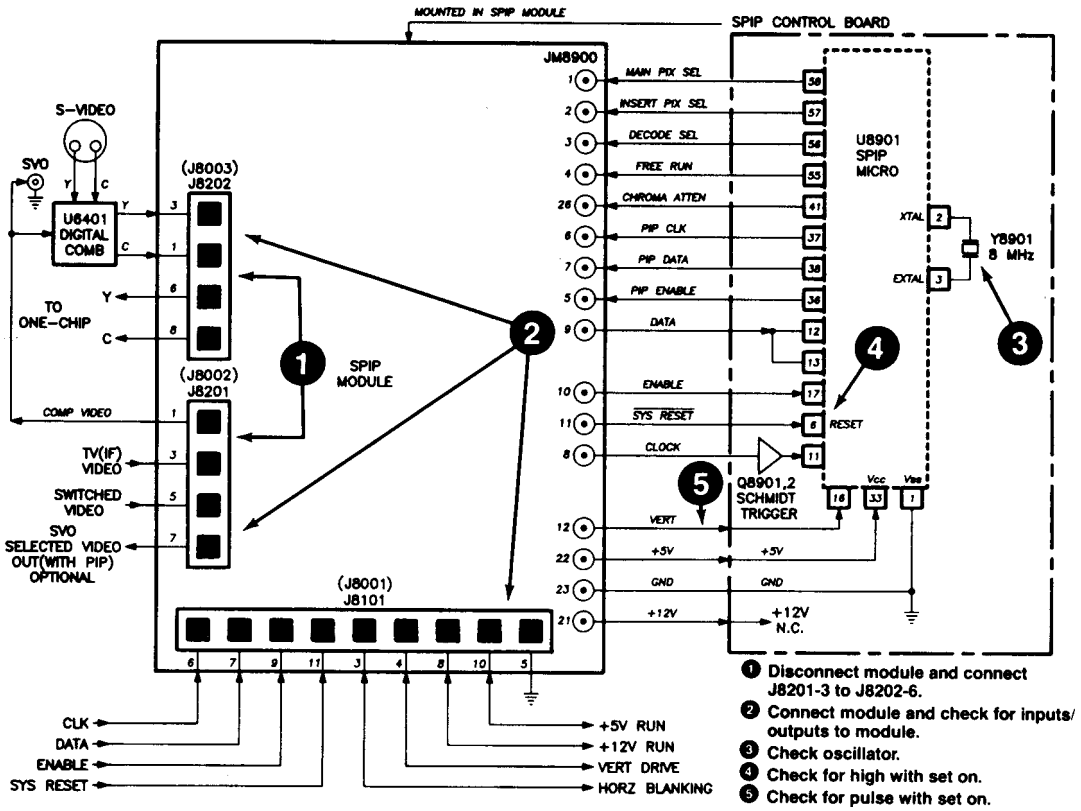


Fig. 35 SPIP Interconnect and Control Board

SPIP Interconnection

Understanding SPIP operation is a little easier if you know how the module is interfaced to the rest of the chassis. The following description explains the signals going to and from the D-SPIP and FF-SPIP modules. The interconnect for the full and defeatured SPIP modules are the same.

In sets with a digital comb filter, all connections to the pip module come from the video features sip board. In sets with an analog comb filter, a pip interconnect board is installed in place of the video features sip to provide connectors for the pip module. The signals going to the pip module are the same regardless of whether the comb is digital or analog. The only thing that changes is the board from which the connectors originate.

Note: Some SPIP modules may have different connector numbers than shown in figure 35. Use the following cross reference or refer to service data for the connector number that applies to the module you are working with.

CONNECTOR	ALTERNATE NAME
J8101	J8001
J8201	J8002
J8202	J8003

External Video Inputs

Composite Video Inputs - J8201

The two composite video inputs to the SPIP module at P8201 are the TV and Switched Video at pins 3 and 5. The TV video input is always from the TV tuner in the chassis. The switched video source is from U1401 of the video input selection circuit and can contain video from either TV, AUX 1, or AUX 2. The signals at these inputs provide the video sources for the big and small pix.

Video Outputs

Composite Video Out - J8201-1

The composite video output signal at J8201-1 is the composite video signal used for the big pix. The signal is applied to the comb filter (in this case digital) to separate it into luma and chroma signals. The composite signal is also routed to the selected video out (SVO) jack on the back of the set.

Y/C Inputs - J8202-3,1

The Y/C signals from the digital comb enter the module at J8202-3 and 1. The S-Video signals are selected by the digital comb filter. Refer to the video input selection section of this manual for S-Video selection with an analog comb filter.

Selected Video Out (with PIP) - J8201-7

The selected video out at J8201-7 may not be implemented in early chassis. Future versions may use this output which is a composite video signal containing both big and small pix information. If available, this signal is applied to the selected video output jack to allow for recording the video signal with PIP onto a VCR or for display on an external monitor. The circuits used to provide this signal may not be populated in the PIP module.

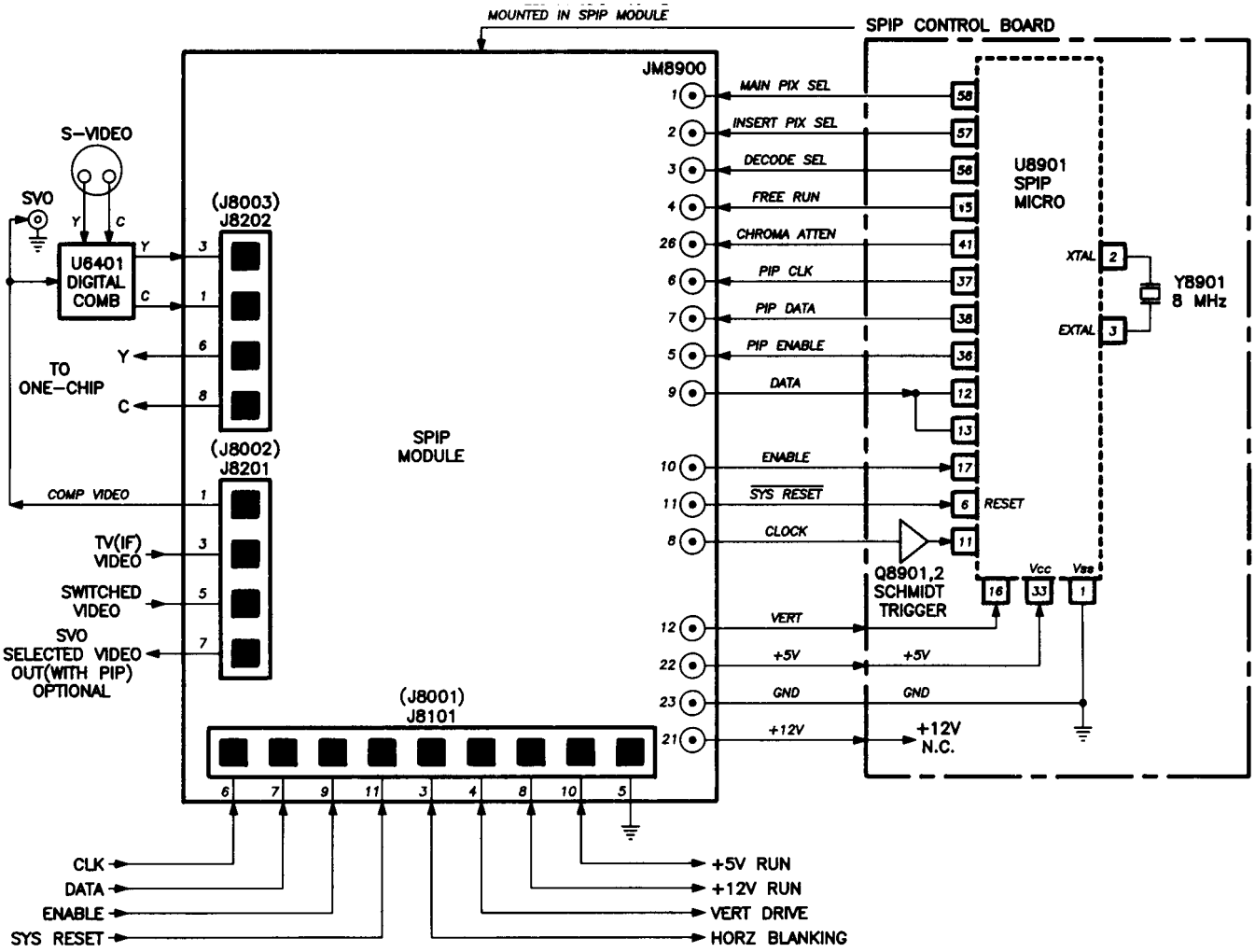


Fig. 35 SPIP Interconnect and Control Board (repeated)

PIP Luma/Chroma Output - P8202-6,8
The luma and chroma signals containing both big and small pix information exit the module at J8202 pins 6 and 8. These signals are applied to the one-chip to produce the big and small picture on the screen.

Control, Power, and Timing Inputs - J8101

Power Supply
Power is provided to the module by the 5 and 12 VDC run supplies at J8101 pins 10, and 8. The supplies are used directly with no regulators in the SPIP module. Always check these supplies when troubleshooting the SPIP module.

H and V Inputs
Both horizontal blanking and vertical reset signals enter the module at J8101 pins 3 and 4. Within the module, horizontal blanking is renamed Flyback and vertical reset is named Vert. Disp. Vertical reset is inverted and routed to the SPIP control micro through JM8900-12. No PIP functions will operate if this signal is missing.

Control Bus
The clock, data, enable, and system reset signals enter the module at J8101. These signals are routed to the SPIP control micro U8901 through JM8900. These signal originate from the system control micro U3101 on the main chassis. All PIP commands are sent to the pip module through this bus. Refer to the system control section of this manual for troubleshooting the activity on these lines. Make sure these four signals are being received by U8901 from pins 8, 9, 10, and 11 of JM8900. If U8901 doesn't receive these signals, no PIP functions can operate.

SPIP Control Micro Board

An additional circuit board containing the SPIP control micro U8901 is housed within the SPIP module. This micro receives PIP commands using the clock, data, and enable lines from the system control micro on the main chassis. The commands are decoded by U8901 and sent to the pip processor U8501 within the module over the PIP Clock, PIP Data, and PIP Enable lines.

Note: When diagnosing a PIP problem, check for activity on the PIP clock, PIP Data, and PIP Enable lines. With the small pix turned off, all lines should be high with no activity. When you turn the small Pix on, all lines should pulse low every 80 milliseconds. Move the time base on your scope to approximately 0.2 msec/divison to see if the lines are swinging from 0 to 5 VDC. If data is not present on these lines, troubleshoot the key signals going to U8901. Loss of vertical reset at pin 16 of U8901 will cause U8901 to never activate the PIP clock, data, and enable lines.

System Reset
U8901 is reset by the system reset line at pin 6. The system reset line is low when the set is off. When the set is first turned on, the system reset line stays low for about 1 second and goes high until the set is turned off. If the system reset line never goes high, U8901 will never execute its program and operate the rest of the PIP module.

U8901 cannot operate if the 8 MHz oscillator at pins 2 and 3 is not operating. Always check the oscillator in addition to checking the reset input at pin 6.

Vertical Reset
The vertical reset signal is inverted and applied to pin 16 of U8901. The micro uses this signal to determine when to send commands to the pip processor in the module. *If this signal is missing, no PIP functions will operate.* With the vertical reset signal missing, the PIP clock, data, and enable lines from U8901 will be inactive when you try to turn pip on.

Switching Control Lines
The Main Pix Select, Insert Pix Select, and Decode Select are control lines used for video switching within the PIP module. These lines are either high or low depending upon the video source selected in the big and small pix.

The Free Run control line goes high during multi-channel mode (FF-SPIP only) to disable various signals in the module. The chroma attenuator line goes high when an external video input is selected for the big pix.

These control lines are covered in more detail in the circuit descriptions in the next few sections of this manual.

PIP Module Verification

Since new modules tend to receive the blame for many TV malfunctions, the following procedure should be used to determine whether the problem is PIP related.

1. Remove AC power from the chassis. Remove all connectors from the PIP module.
2. Jumper the TV video signal at J8201-3 (P6402) to the luma J8202-6 (P6401) and chroma J8202-8 (P6401) inputs to the one-chip. This bypasses the video switching within the PIP module.
3. Turn the set on. You should see a color picture since we jumpered the composite TV video signal to the luma and chroma inputs of the one-chip. The picture quality may not be perfect since we are jumpering composite video into points which require component luma and chroma signals.

If the problem still exists after bypassing the module, troubleshoot the chassis since the PIP module is probably not causing the problem.

If the problem did disappear after bypassing the PIP module, you *CANNOT* assume the PIP module is defective until you have verified signals going to and from the module. There are some cases where loss of external signals to the module make it appear to be defective when it really isn't. If the signals going to the module appear to be OK, begin troubleshooting to the component level inside the module.

PIP Module Troubleshooting

Symptom: No PIP functions, normal picture OK.

1. Always check signals on connectors J8201, J8202, and J8101 before getting into the module. If they are OK, go to step 2.
2. Check for vertical pulse at pin 16 of U8901. If present, go to step 3.
3. Check for high on reset pin 6 of U8901 and for 8 MHz oscillator at pin 2 and 3 of U8901. If present, go to step 4.
4. Check for low going pulses on PIP clock, data, and enable lines from U8901 when attempting to turn on small pix. If present, the problem is probably on the main board of the PIP module.

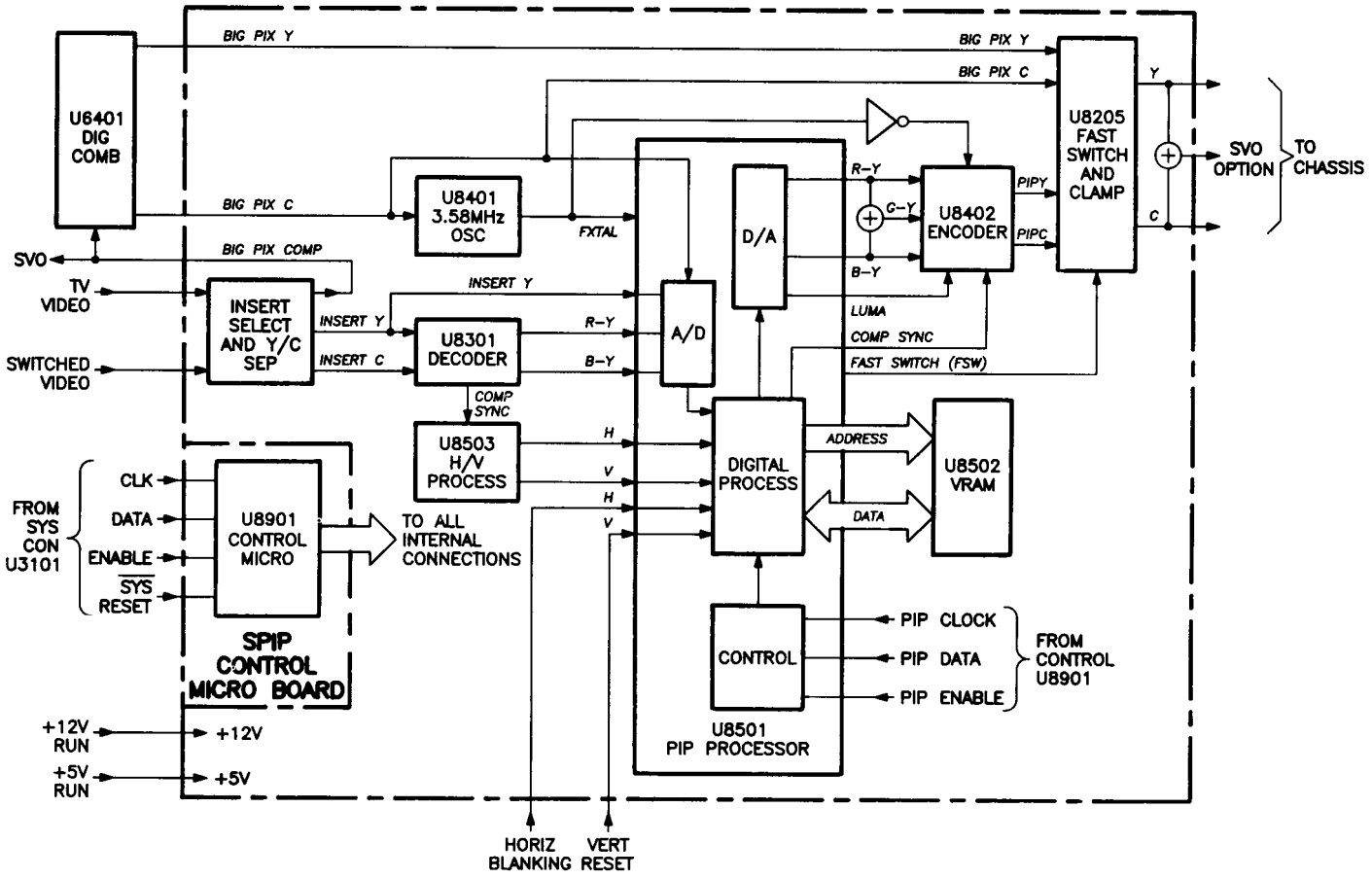


Fig. 36 SPIP Module Block Diagram

SPIP Module Block Diagram

The block diagram in Figure 36 shows the basic circuits contained within the SPIP Module.

Input Selection and Y/C Separation

This stage selects the desired video source to fill the big and small pix viewed on the screen. The TV Video and Switched Video inputs are composite and must be separated into component luminance and chrominance signals. The main pix video Y/C separation is performed by the digital (or analog) comb on the main chassis while the insert pix is separated within the SPIP module. The main pix Y/C signals from the external comb enter the module for application to the fast switch and 3.58 MHz oscillator, and PIP processor stages. The insert Y/C signals are applied to the decoder stage and the PIP processor.

Y/C to R-Y/B-Y Decoder

The insert luma and chroma signals enter the decoder stage consisting of U8301 for conversion into R-Y and B-Y color difference signals for application to the PIP Processor U8501. Composite sync is separated from the luminance signal and is applied to the H and V processing stage. Note that the PIP Y signal is also applied directly to the PIP Processor.

3.58 MHz Oscillator - U8401

The 3.58 MHz oscillator provides a continuous 3.58 MHz signal to the Encoder stage and to the PIP processor. The oscillator is locked to the color burst of the big pix chroma signal. During Multi-Channel mode (FF-SPIP only), the oscillator is forced to free run because the color burst changes for each of the twelve channels displayed on the screen.

The PIP processor uses the 3.58 MHz signal during Multi-Channel mode to phase lock its 20 MHz VCO. The Encoder U8402 uses the signal to produce the 3.58 MHz chroma signal for the output stage.

H/V Sync Signals

The horizontal and vertical sync outputs of the H and V processor stage are locked to the composite sync output of the Decoder stage. The H and V processor free runs in the absence of composite sync to maintain H and V pulses to the PIP processor. These sync signals are used by the pip processor to time the writing of insert pix video information to the VRAM.

Horizontal and Vertical sync pulses from the TV Deflection circuits are also applied to the PIP Processor. The PIP processor contains a voltage controlled 20 MHz

oscillator to synchronize its internal timing with external horizontal sync signals. When the small pix is turned on, horizontal from the chassis deflection circuit is compared to an internally generated phase reference to produce the error voltage for the VCO. During full field effects such as Freeze or Zoom, H sync from the H/V processor is used. During Multi Channel mode, 3.58 MHz (FXTAL) from the oscillator U8401 is divided down within the PIP processor to be used as the input to the phase detector circuit.

The horizontal blanking and vertical reset signals from deflection are also used by the PIP processor as timing signals to read small pix information from the VRAM.

PIP Processor (U8501)

Analog to Digital Conversion
The Analog to Digital converter within the PIP Processor U8501 converts the analog PIP Luma, B-Y, and R-Y signals into digital information. The big pix chroma signal is used as a reference to establish the chroma level for the small pix.

Digital Processing and Control
The digital processing stage receives the digital video information from the A/D converter and stores two fields of video into the VRAM U8502. Once in RAM, the digital data can be recalled and manipulated by the Digital Processing stage.

The Control Stage receives commands from the control micro U8901 through the three wire serial communications bus consisting of PIP Clock, Data, and Enable. The control stage manages the functions of the Digital Processing Stage to produce the various PIP features and functions. The initial PIP commands come from the system control micro U3101 on the chassis through the clock, data, and enable lines as show on the left side of figure 36.

Digital To Analog Conversion
The manipulated digital data from the Digital Processing Stage enters the D/A converter to produce the analog Luma, R-Y and B-Y signals that are fed to the output stages of the SPIP module. These video signal contain the information of the small pix. During full field effects such as freeze or zoom (FF-SPIP only), these signals are used to produce the picture on the entire screen.

R-Y, B-Y to Y/C Encoder (U8402)

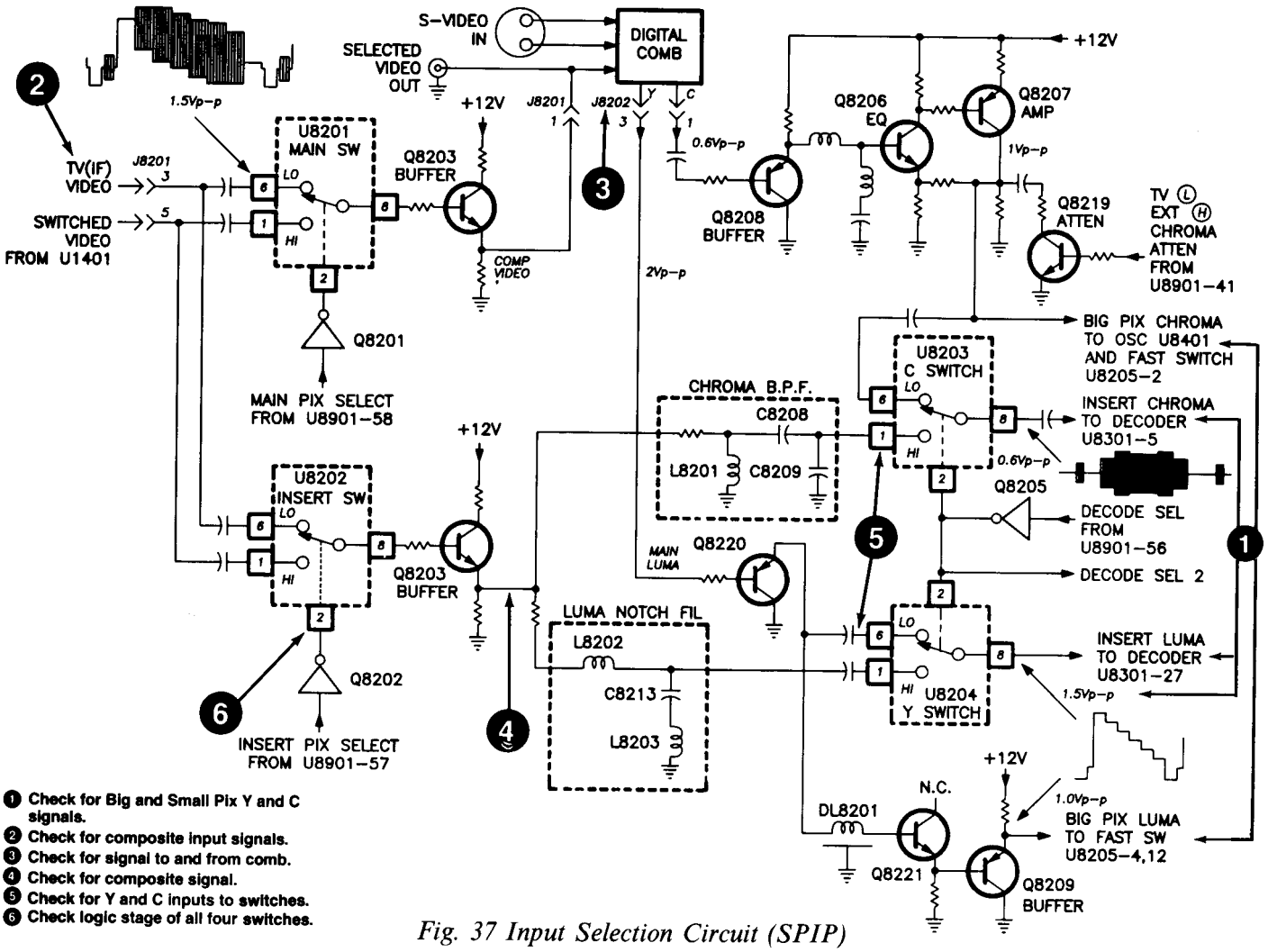
The Encoder U8402 receives the Luma, R-Y, B-Y, and G-Y (derived from R-Y and B-Y) signals from the PIP Processor and produces a 3.58 MHz PIP chroma signal and a PIP luminance signal containing composite sync. The 3.58 MHz signal used for the R, G, B-Y to chroma conversion is the inverted FXTAL signal from U8401.

Fast Switch (U8205) and Output

The Fast Switch U8208 takes the PIP Y/C signals from the Encoder and mixes them (by switching) into the Big Pix Y/C signals to create the video signal that is viewed on the screen. The Fast Switch control line inserts (switches) each line of the small pix video into the appropriate line of the big pix video.

The fast switch is also responsible for clamping the back porch blanking level of the small pix luma signal to the blanking level of the big pix.

The Y/C output of the Fast Switch is applied to the Y and C inputs of the one chip to produce the big and small pix images on the screen. Some future versions of SPIP may combine the Y and C signals to provide a composite video signal containing both big and small pix information to the selected video output jack on the back of the set. The circuit needed to perform this mixing may not be populated in current SPIP modules.



1. Check for Big and Small Pix Y and C signals.
2. Check for composite input signals.
3. Check for signal to and from comb.
4. Check for composite signal.
5. Check for Y and C inputs to switches.
6. Check logic stage of all four switches.

Fig. 37 Input Selection Circuit (SPIP)

SPIP Input Selection Circuit

Figure 37 shows the input selection circuits used within the SPIP module. The functions of this stage are:

1. Select the composite video source for the main (big) and the insert (small) pix.
2. Separate the composite video sources for the big and small pix into separate Y and C signals.
3. Select the desired small pix Y and C signals to be used to produce the small pix.

The two composite video inputs to the module at J8201 are the TV and Switched Video signals at pins 3 and 5. The TV video input is always from the TV tuner in the chassis. The switched video source is from U1401 of the video input selection circuit and can contain video from either the TV Tuner, Input 1, or Input 2.

Big Pix Signal Path (TV Video)

Main (Big) Pix Composite Source Selection

The main (big) pix signal is selected by switch U8201. It selects either the video from the TV tuner or one of the sources from switched video U1401 on the chassis. Switch U8201 is controlled at pin 2 by the inversion of the Main Pix Select line from the SPIP control micro U8901. A high at pin 2 selects the switched video source while a low selects the TV tuner.

The following chart lists the logic level of the Main Pix select line at U8901-58 under various modes of PIP operation.

Main Pix	Insert Pix	Main Pix Select
Tuner	OFF	Low
Tuner	Tuner	High
Tuner	EXT	High
EXT	OFF	Low
EXT	Tuner	Low

Big Pix Luma/Chroma Separation

The output of the switch U8201 is buffered by Q8203 and applied to the input of the comb filter (either digital or analog) on the chassis. The signal is also applied to the selected video output jack on the back of the set. Notice that no PIP information is present in the selected video output when taken from this point.

The Y and C signals from the comb enter the module at J8203 pins 3 and 1. The chroma signal is buffered, equalized and amplified by Q8206, 7, and 8 before being applied to the chroma switch U8203. The chroma attenuator line from the SPIP control micro U8901 goes high whenever the big pix chroma is from an external video input as opposed to the TV tuner. The high turns on Q8219 to decrease the amplitude of the chroma signal to the same level as received from TV tuner. After the chroma attenuator, the chroma signal is also applied to the 3.58 MHz oscillator U8401 and the fast switch U8205.

The luma signal from the comb is buffered by Q8220 and applied to luma switch U8204 pin 6 and also to delay line DL8201. The output of the delay line passes through diode Q8221 and is buffered by Q8209 for application to the fast switch U8205.

The chroma signal at the collector of Q8207 is labeled Big Pix Chroma while the luma signal at the emitter of Q8209 is labeled Big Pix Luma. From this point on, the big pix Y and C signals go relatively unaltered (except for fast switching) to the output of the pip module for application to the one chip. In D-SPIP modules, these signals will always be used to produce the big pix information on the screen since D-SPIP contains no full field special effect such as zoom or multi channel.

In FF-SPIP applications during freeze or zoom, the big picture is actually digitized information whose Y/C source must pass through the pip processor via the outputs of U8203 and U8204.

S-Video Selection
In sets with digital comb filters, both the S-Luma and S-Chroma signals are selected by the comb filter. In sets analog combs, S-Chroma selection is performed by U1401 while the S-Luma is selected on the DPIP adaptor board. In either application, the S-Video signals enter the PIP module at J8202 Pins 3 and 1.

Note: The composite video from an S-Video device must be plugged into its assigned video input on the back of the TV in addition to the S-Video connector. The Y/C signals from the S-Video connector cannot be applied to the small pix when the TV tuner is in the big pix. The composite signal from the S-Video device must be used in this case.

Insert (Small) Pix Signal Path

Small Pix Composite Source Selection
The Insert Switch U8202 selects the video source for the Insert (small) pix from either the composite TV tuner signal or from the switched video source from U1401 on the chassis. Switch U8201 is controlled at pin 2 by the inversion of the Insert Pix Select line from the SPIP control micro U8901-57. A high at pin 2 selects the switched video source while a low selects the TV tuner.

The following chart lists the logic level of the Insert Pix Select line at U8901-57 under various modes of PIP operation.

Main Pix	Insert Pix	Insert Pix Select
Tuner	OFF	High
Tuner	Tuner	High
Tuner	EXT	Low
EXT	OFF	Low
EXT	Tuner	High

Small Pix Y/C Separation
The output of PIP Switch U8202 is buffered by Q8203 before being applied to Chroma Band Pass Filter L8201 and Luma Notch Filter L8202. These filters separate the composite video signal into separate luma and chroma signals just as the comb filter did in the main pix signal path. These filters are used instead of a comb because a wide luminance bandwidth is not necessary due to the limited resolution requirements of the small pix.

Decode Select Line
The output of Chroma BPF is applied to switch U8203-1 and the output of the luma notch filter is applied to switch U8204-1. The other inputs to the switch ICs are the Big Pix luma and chroma signals from the comb filter. The inversion of the Decode Select line from the SPIP control micro U8901-56 controls switch U8203 and U8204 to select between the two luma/chroma sources.

When the small pix insert is enabled, the Decode Select line goes low to select the luma/chroma signals from the BPF and notch filters. Whenever you do a full field special effect such as Freeze or Zoom (FF-SPIP only), Decode Select goes high to select the luma/chroma from the comb filter to obtain better luminance resolution provided by the comb.

The Decode select line in the D-SPIP module remains low at all times to select only the Y/C signals from the chroma band pass filter and luma notch filter since there are no full field effects in this module.

The decode select line is inverted by Q8205 to create the decode select 2 line which is used by the anti-aliasing filter on the R-Y/B-Y signals covered in the next section of this manual.

Note: All PIP features including full field effects (FF-SPIP only) use the video sources from the outputs of U8203 and U8204 to create the small pix or a digitized full field effect. These signals are decoded and supplied to the PIP processor U8501 to be digitized for the desired PIP feature. If no video appears in the small pix or during a full field effect, begin troubleshooting by checking for Y/C signals from these switches.

Input Selection Troubleshooting

Symptom - No big or small pix Video

1. Check for Insert Y/C signals from U8203, and U8204. Also check for Big Pix luma and chroma signals at the output of the input selection stages. If all signals are present, the Input selection stage is probably not the problem. If not present, go to step 2.
2. Check for composite video at TV and Switched video inputs at J8201 pins 3 and 5. If present, go to step 3.
3. Trace composite video from U8201 to comb filter and trace output of comb through input selection stages. Also trace insert composite signal from U8202 through Chroma BPF and Luma notch filter to Y and C switches U8203 and 4. Also check for proper logic levels at switching ICs.

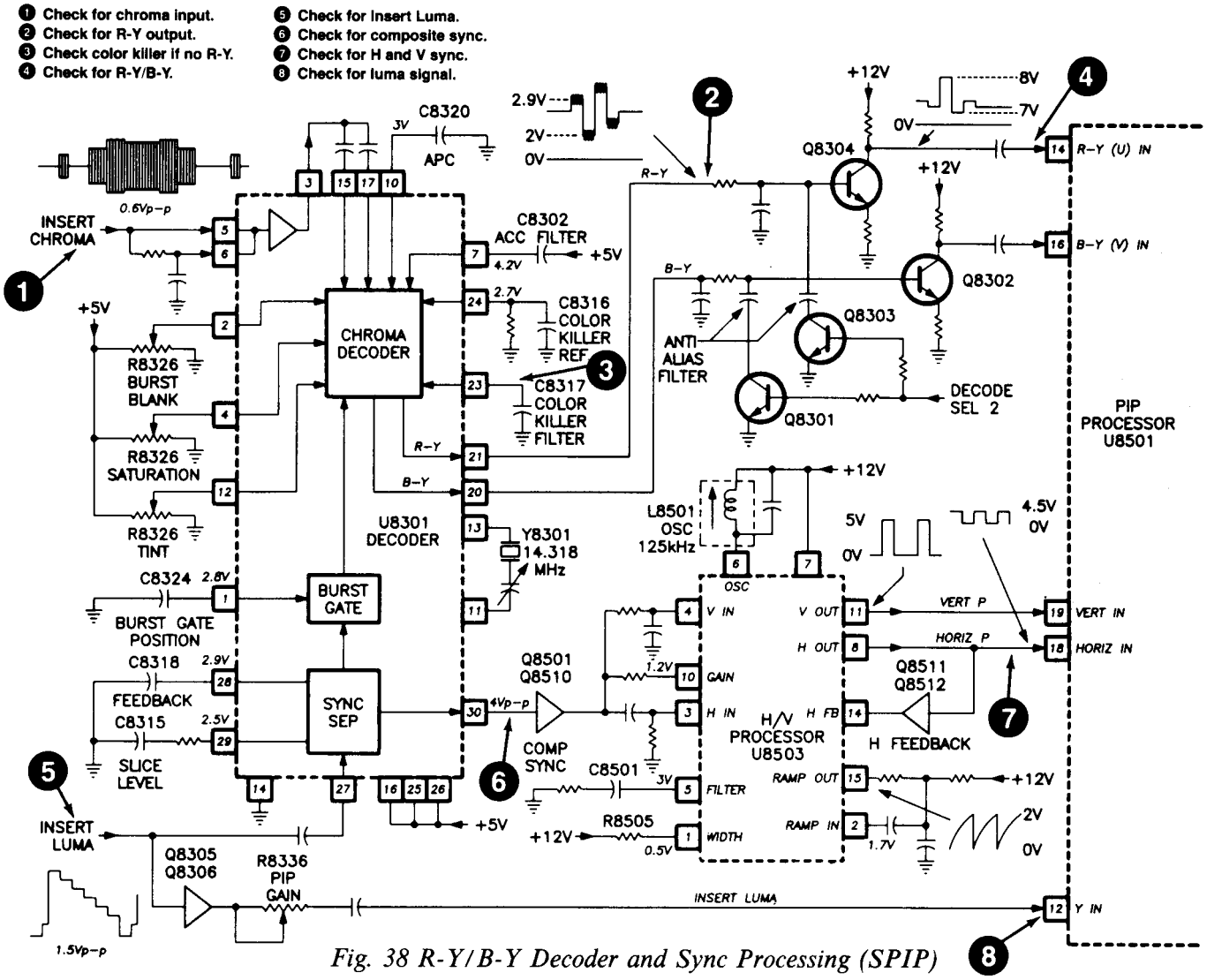


Fig. 38 R-Y/B-Y Decoder and Sync Processing (SPIP)

Y/C Decoding and Sync Processing

The purpose of this stage:

1. Convert the Insert (small pix) chroma signal to R-Y and B-Y color difference signals for application to the PIP processor U8501 for digitization.
2. Apply the insert Luma signal to the PIP processor U8501 for digitization.
3. Provide the PIP processor U8501 separate horizontal and vertical sync signals from the insert luma signal.

Y/C Decoder - U8301

U8203 and U8204 in the Input Selection stage provide the luminance and chrominance signals for the PIP processor to create the small pix and full field special effects. The PIP Processor U8501 requires R-Y and B-Y color difference signals instead of the 3.58 MHz chroma signal. The Decoder U8301 converts the chroma signal to the R-Y and B-Y format.

Insert Chroma
Pins 5 and 6 of U8301 receive the Insert (small) Chroma signal from the input selection stage. The chroma signal is buffered within U8301 and exits at pin 3 where it is capacitively coupled back into the IC at pins 15 and 17. The signal enters the chroma processing stage where the conversion to R-Y and B-Y occurs. The APC capacitor at pin 10 of U8301 provides automatic phase control of the chroma signal during the decoding process. The ACC filter at pin 7 maintains constant chroma level.

Color Killer
If the level of the chroma burst is low or missing, the color killer circuit turns off the decoding process to stop production of the R-Y or B-Y signals. When the color killer filter voltage at pin 23 reaches the color killer reference voltage at pin 24, the color killer circuit activates. Normally the filter voltage at pin 23 is around 2 VDC. As chroma burst level decreases, the voltage at pin 23 increases. When it reaches the reference of about 2.7 VDC, the color killer activates.

This is not the only stage in the PIP module that could cause loss of chroma. If the big pix signal doesn't contain a color burst, the small pix chroma will not contain chroma information either. However there will still be R-Y and B-Y outputs from U8301. This will be explained in the PIP Processor section of this manual.

Burst Gate
The burst gate for the chroma demodulation is received from the internal sync separator within U8301. Sync is removed from insert luma signal to produce the burst gate. The burst gate position is controlled by C8324 at pin 1. Normally the voltage at pin 1 is about 2.8VDC. If the capacitor at pin 1 shorts or opens, the small pix looses chroma sync producing unstable chroma patterns in the small pix.

R-Y/B-Y Outputs
The R-Y and B-Y color difference signals from U8301 exit at pins 21 and 20. The decoder's master oscillator at pins 11 and 13 operates at 14.318 MHz. The high frequency oscillator components are removed from the R-Y and B-Y signals before being inverted by Q8302 and Q8304. After the inversions, the signals are applied to the PIP processor U8501 where they will be converted into digital information and stored in the VRAM.

The *Saturation* control R8342 adjusts the color level or saturation of the small pix while the *Tint* control R8307 adjust the hue or tint.

The Burst Blank adjustment R8236 removes the color burst from the R-Y and B-Y outputs of the decoder. If this control is not adjusted properly, you will not be able to obtain the correct small pix tint when adjusting the *Tint* control R8307.

Anti-Alias Filtering
When the small pix is turned on, the Decode Select 2 line goes high to turn on Q8301 and Q8303. This switches the anti-aliasing filter caps to ground, limiting the bandwidth of the R-Y and B-Y signals. This prevents alias signals from being produced in the small pix. Alias signals are produced when the input signal frequency is equal to or greater than the sampling frequency of the A/D converter within the PIP processor.

Sync Separator
The insert (PIP) luma from the input selection stage enters the sync separator in U8301 at pin 27. The insert luma signal is buffered by Q8305 and Q8306 and level adjusted by R8336 before entering the PIP Processor at pin 12.

Sync is removed from the insert luma signal to create a composite sync output at U8301-30. Two external pins for the sync separator are the feedback and slice level controls at pins 28 and 29. The feedback control affects the gain of the stage while the slice level controls the voltage where sync is stripped from the luma signal. The voltage at these pins is normally about 2.9 VDC at the feedback control and about 2.5 VDC at the slice level control.

Sync Processing

H and V Processor - U8503
The composite sync output of Decoder U8301 is buffered by Q8501 and Q8510 before being applied to the H and V Processor U8503. The H/V Processor produces separate horizontal and vertical sync outputs which are locked to the incoming composite sync signal. U8503 is merely a countdown deflection IC used in previous RCA CTC131 chassis.

The horizontal portion of the composite sync signal is applied to pin 3 while the vertical component is integrated and applied to pin 4. The gain control at pin 10 controls the gain of the H and V sync inputs at pins 3 and 4.

The oscillator at pin 6 operate at about 8 times horizontal. The oscillator is part of an internal VCO which compares the phase of incoming horizontal with a divided down reference. The error voltage is filtered at pin 5 of U8503. The phase locked divided down reference produces the horizontal ramp at pin 15 and 2. The ramp is locked to the horizontal sync input at pin 3 to produce the horizontal output at pin 8.

The width control at pin 1 affects the burst gate pulse generator within the IC. The burst gate is not used in this application. The feedback at pin 14 is also used by a horizontal blanking circuit which is not used in this application. Although neither signals are used, the pins must be set up as shown.

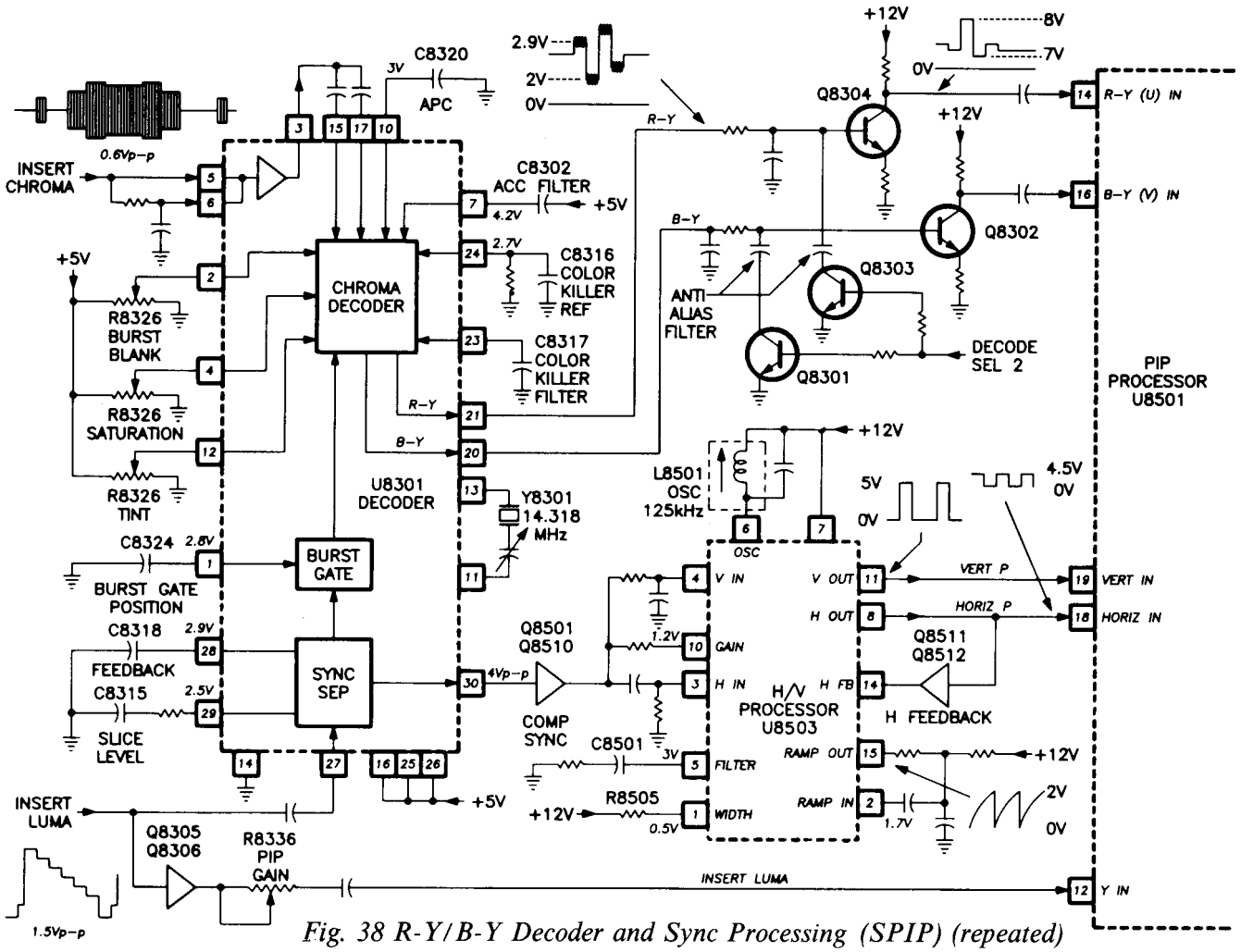


Fig. 38 R-Y/B-Y Decoder and Sync Processing (SPIP) (repeated)

The vertical output is also derived from a countdown of the oscillator at pin 8. The vertical countdown circuit is reset by vertical sync at pin 4. In the absence of composite sync, U8503 free runs to maintain horizontal and vertical sync pulses at its output pins 8 and 11.

L8501 is used to adjust the free run frequency of U8503 during loss of composite sync. If the border of the small pix is stable on the screen but the video content of the small pix is rolling vertically or tearing horizontally, check the H and V outputs of U8503 or the adjustment of L8501.

To verify that the H and V signals from pins 8 and 11 of U8503 are locked to the insert luma signal, place the insert luma signal and one or both of the H and V signals on a scope. Trigger the scope on the sync signal. The two signals should be locked together.

Troubleshooting

Symptom: Small Pix Color and Tint don't match Big Pix.

1. Adjust SAT and TINT controls at U8301.
2. If small pix cannot be adjusted correctly, verify proper setting of Burst Blank adjustment. Also check APC cap at UK8301-10.

Symptom: Small Pix chroma not in sync.

1. Check burst gate DC voltage at U8301-1 and check C8324.

Symptom: No small pix chroma.

1. Verify chroma input at U8301-5,6. If present, check for B-Y and R-Y outputs at U8301-20,21. Make sure big pix is a color signal. If not, the small pix will also be monochrome.
2. Check 14.318 MHz oscillator.
3. Check color killer reference and killer filter voltage. Also check ACC and APC filter caps at U8301-10, 7.

Symptom: Small pix takes time to lock horizontally.

1. Verify adjustment of L8501 on U8503.

Symptom: Small pix rolls vertically or tears horizontally within pix border. Insert border is stable on screen.

1. Check for H and V outputs of U8503-8, 11. If present, check for H and V inputs at U8503-3, 4. Check for composite sync at output of U8301-30.
2. Check for H ramp at U8503-15. Also check other DC voltages and signals on pins of U8503.

Insert Chroma
Pins 5 and 6 of U8301 receive the Insert (small) Chroma signal from the input selection stage. The chroma signal is buffered within U8301 and exits at pin 3 where it is capacitively coupled back into the IC at pins 15 and 17. The signal enters the chroma processing stage where the conversion to R-Y and B-Y occurs. The APC capacitor at pin 10 of U8301 provides automatic phase control of the chroma signal during the decoding process. The ACC filter at pin 7 maintains constant chroma level.

Color Killer
If the level of the chroma burst is low or missing, the color killer circuit turns off the decoding process to stop production of the R-Y or B-Y signals. When the color killer filter voltage at pin 23 reaches the color killer reference voltage at pin 24, the color killer circuit activates. Normally the filter voltage at pin 23 is around 2 VDC. As chroma burst level decreases, the voltage at pin 23 increases. When it reaches the reference of about 2.7 VDC, the color killer activates.

This is not the only stage in the PIP module that could cause loss of chroma. If the big pix signal doesn't contain a color burst, the small pix chroma will not contain chroma information either. However there will still be R-Y and B-Y outputs from U8301. This will be explained in the PIP Processor section of this manual.

Burst Gate
The burst gate for the chroma demodulation is received from the internal sync separator within U8301. Sync is removed from insert luma signal to produce the burst gate. The burst gate position is controlled by C8324 at pin 1. Normally the voltage at pin 1 is about 2.8VDC. If the capacitor at pin 1 shorts or opens, the small pix looses chroma sync producing unstable chroma patterns in the small pix.

R-Y/B-Y Outputs
The R-Y and B-Y color difference signals from U8301 exit at pins 21 and 20. The decoder's master oscillator at pins 11 and 13 operates at 14.318 MHz. The high frequency oscillator components are removed from the R-Y and B-Y signals before being inverted by Q8302 and Q8304. After the inversions, the signals are applied to the PIP processor U8501 where they will be converted into digital information and stored in the VRAM.

The *Saturation* control R8342 adjusts the color level or saturation of the small pix while the *Tint* control R8307 adjust the hue or tint.

The Burst Blank adjustment R8236 removes the color burst from the R-Y and B-Y outputs of the decoder. If this control is not adjusted properly, you will not be able to obtain the correct small pix tint when adjusting the *Tint* control R8307.

Anti-Alias Filtering
When the small pix is turned on, the Decode Select 2 line goes high to turn on Q8301 and Q8303. This switches the anti-aliasing filter caps to ground, limiting the bandwidth of the R-Y and B-Y signals. This prevents alias signals from being produced in the small pix. Alias signals are produced when the input signal frequency is equal to or greater than the sampling frequency of the A/D converter within the PIP processor.

Sync Separator
The insert (PIP) luma from the input selection stage enters the sync separator in U8301 at pin 27. The insert luma signal is buffered by Q8305 and Q8306 and level adjusted by R8336 before entering the PIP Processor at pin 12.

Sync is removed from the insert luma signal to create a composite sync output at U8301-30. Two external pins for the sync separator are the feedback and slice level controls at pins 28 and 29. The feedback control affects the gain of the stage while the slice level controls the voltage where sync is stripped from the luma signal. The voltage at these pins is normally about 2.9 VDC at the feedback control and about 2.5 VDC at the slice level control.

Sync Processing

H and V Processor - U8503
The composite sync output of Decoder U8301 is buffered by Q8501 and Q8510 before being applied to the H and V Processor U8503. The H/V Processor produces separate horizontal and vertical sync outputs which are locked to the incoming composite sync signal. U8503 is merely a countdown deflection IC used in previous RCA CTC131 chassis.

The horizontal portion of the composite sync signal is applied to pin 3 while the vertical component is integrated and applied to pin 4. The gain control at pin 10 controls the gain of the H and V sync inputs at pins 3 and 4.

The oscillator at pin 6 operate at about 8 times horizontal. The oscillator is part of an internal VCO which compares the phase of incoming horizontal with a divided down reference. The error voltage is filtered at pin 5 of U8503. The phase locked divided down reference produces the horizontal ramp at pin 15 and 2. The ramp is locked to the horizontal sync input at pin 3 to produce the horizontal output at pin 8.

The width control at pin 1 affects the burst gate pulse generator within the IC. The burst gate is not used in this application. The feedback at pin 14 is also used by a horizontal blanking circuit which is not used in this application. Although neither signals are used, the pins must be set up as shown.

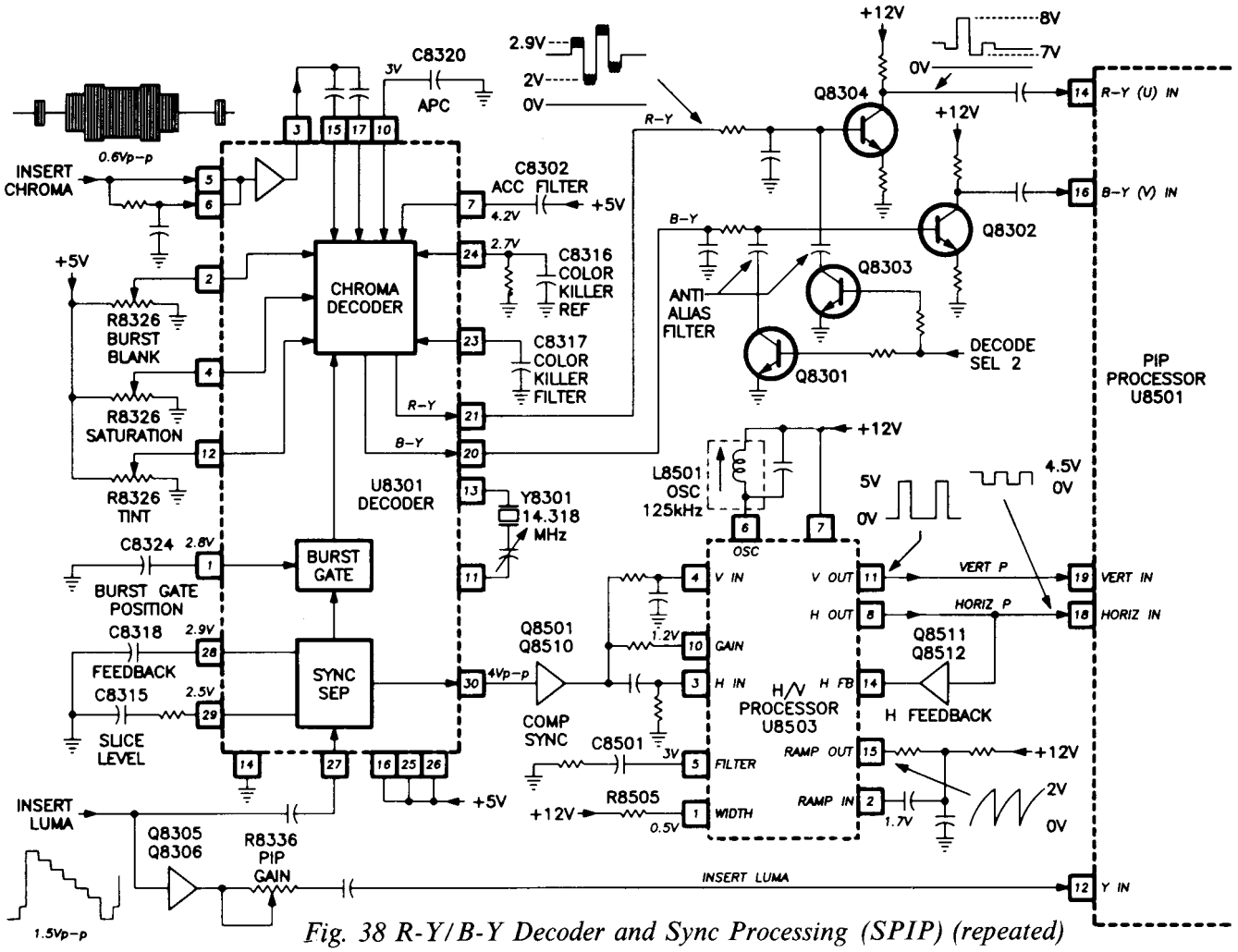


Fig. 38 R-Y/B-Y Decoder and Sync Processing (SPIP) (repeated)

The vertical output is also derived from a countdown of the oscillator at pin 8. The vertical countdown circuit is reset by vertical sync at pin 4. In the absence of composite sync, U8503 free runs to maintain horizontal and vertical sync pulses at its output pins 8 and 11.

L8501 is used to adjust the free run frequency of U8503 during loss of composite sync. If the border of the small pix is stable on the screen but the video content of the small pix is rolling vertically or tearing horizontally, check the H and V outputs of U8503 or the adjustment of L8501.

To verify that the H and V signals from pins 8 and 11 of U8503 are locked to the insert luma signal, place the insert luma signal and one or both of the H and V signals on a scope. Trigger the scope on the sync signal. The two signals should be locked together.

Troubleshooting

Symptom: Small Pix Color and Tint don't match Big Pix.

1. Adjust SAT and TINT controls at U8301.
2. If small pix cannot be adjusted correctly, verify proper setting of Burst Blank adjustment. Also check APC cap at UK8301-10.

Symptom: Small Pix chroma not in sync.

1. Check burst gate DC voltage at U8301-1 and check C8324.

Symptom: No small pix chroma.

1. Verify chroma input at U8301-5,6. If present, check for B-Y and R-Y outputs at U8301-20,21. Make sure big pix is a color signal. If not, the small pix will also be monochrome.
2. Check 14.318 MHz oscillator.
3. Check color killer reference and killer filter voltage. Also check ACC and APC filter caps at U8301-10, 7.

Symptom: Small pix takes time to lock horizontally.

1. Verify adjustment of L8501 on U8503.

Symptom: Small pix rolls vertically or tears horizontally within pix border. Insert border is stable on screen.

1. Check for H and V outputs of U8503-8, 11. If present, check for H and V inputs at U8503-3, 4. Check for composite sync at output of U8301-30.
2. Check for H ramp at U8503-15. Also check other DC voltages and signals on pins of U8503.

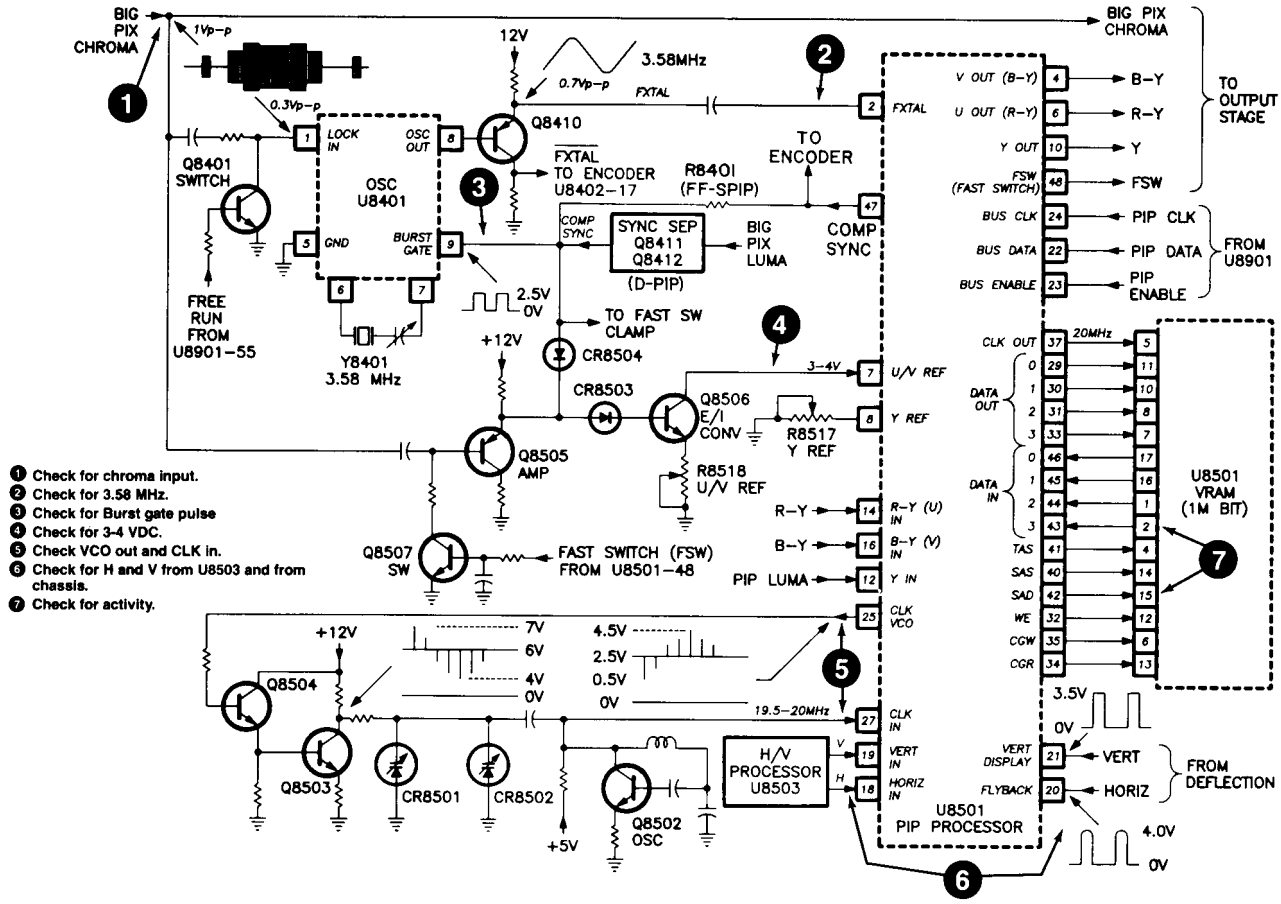


Fig. 39 SPIP Processor

PIP Processor U8501

PIP Processor Stage Functions:

1. Phase lock the master VCO to the horizontal sync signal from U8503, from the chassis, or from the divided FXTAL signal depending upon the mode of operation.
2. Determine the small pix chroma level from the big pix chroma reference.
3. Receive operational commands from U8901 through the PIP clock, data, and enable lines to execute the desired PIP feature and various operational instructions.
4. Store the digitized small pix video data in VRAM and retrieve it and convert it to analog R-Y/B-Y and luma signals along with a fast switch signal to insert them into the big pix for application to the output stage of the PIP module.

VCO Master Oscillator and H/V Sync

The main oscillator at pin 27 of PIP Processor U8501 runs at 19.5 to 20.7 MHz. The oscillator consists of varactor diode CR8501,2 and Q8502. The frequency of oscillation is controlled by the DC voltage applied to CR8501,2 from the CLK VCO output at U8501-25.

This VCO is part of a PLL which synchronizes the master oscillator with incoming H sync at pin 18 during full field effects (FF-SPIP only), Deflection H sync during small pix operations, and FXTAL during Multi-Channel mode (FF-SPIP only). Since sync is unstable during Multi-Channel mode, the CAV micro instructs the PIP processor to uses 3.58 MHz FXTAL signal at pin 2 (internally divided down to 15,734 Hz) instead of the H sync input at pin 18.

One of the three horizontal signals described in the previous paragraph is applied to an internal phase detector which compares it to a reference signal generated within the pip processor. The error pulse from the phase detector exit U8501 at pin 25. The pulses are buffered and inverted by Q8504 and Q8503 to control the voltage on the varactor diodes CR8501 and CR8502. Their capacitance affects the frequency of oscillation of Q8502 until the PLL is locked to the horizontal sync reference.

The H and V signals from U8503 applied to pins 18 and 19 of the PIP processor are used as timing signals to determine when to write video data *into* the VRAM. The H and V signals from the deflection circuits are used to synchronize the reading of video data *from* the VRAM. Loss of any of these signals will cause PIP functions to malfunction as described below.

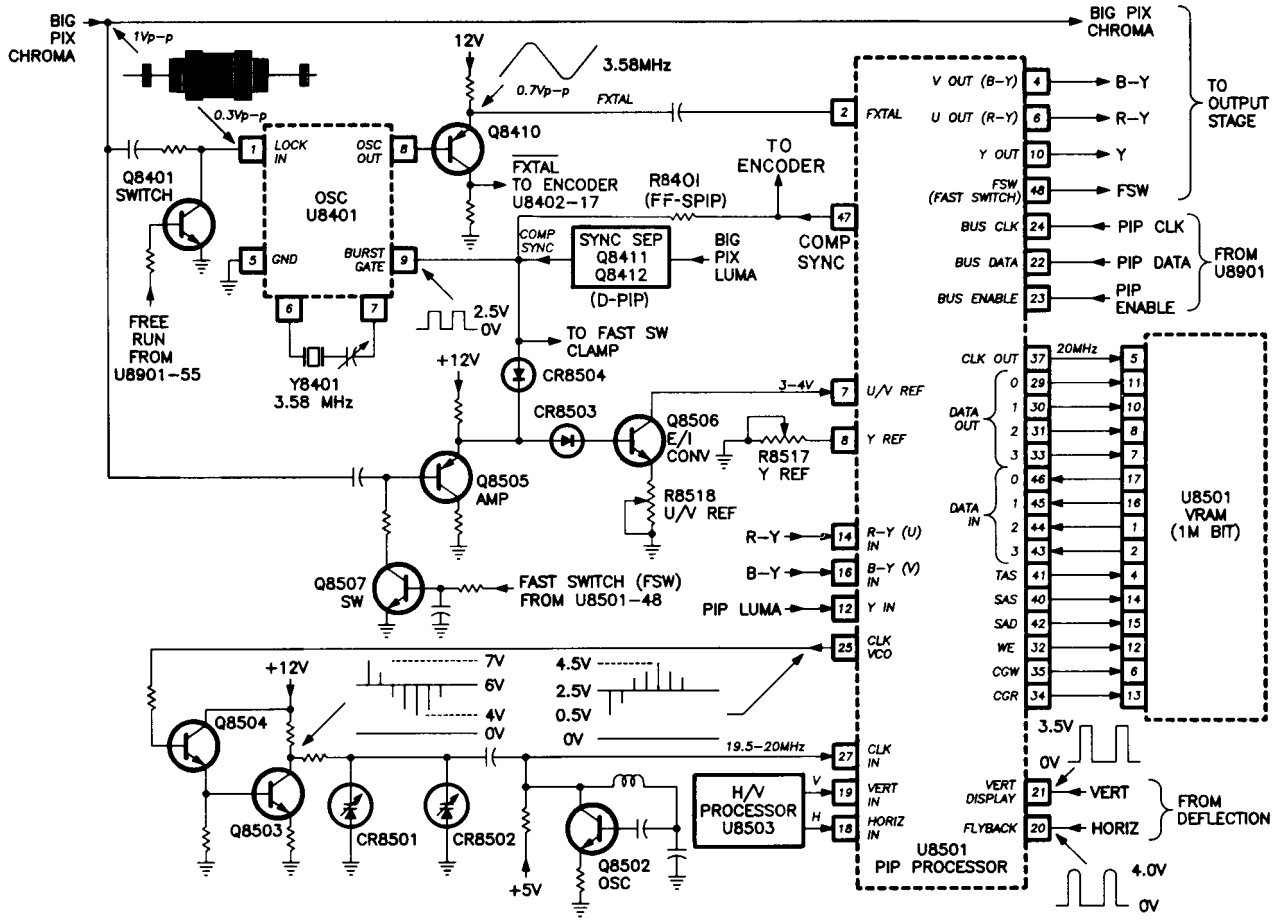


Fig. 39 SPIP Processor (repeated)

Troubleshooting Tips

Signal Lost	*Resulting Symptom*
H at Pin 18	Small pix is black with no video.
H at Pin 20	Big pix normal, small pix tears across width of screen.
V at Pin 19	White bars in big pix with no video with all PIP functions disabled.
V at Pin 21	Small pix rolls vertically through big pix and cannot be turned off.

3.58 MHz Oscillator U8401

U8401 produces a continuous 3.58 MHz sine wave for the PIP Processor and the Encoder stage. During all modes of operation except multi channel mode (FF-SPIP only), the 3.58 MHz output of U8401 is phase locked to the color burst of the Big Pix chroma signal at pin 1. The burst gate signal at pin 9 allows only the burst portion of the Big Pix chroma signal to affect the phase locking operation. Without the burst gate signal, chroma sync will be lost in the small pix.

The burst gate at pin 9 of U8401 is derived the sync of the big pix luma in D-SPIP and from the composite sync output of U8501-47 in the FF-SPIP. In the FF-SPIP, R8401 will be inserted to provide the burst gate from U8501-47 while the output of sync separator Q8411 and Q8412 will be disabled.

The FXTAL signal is used by the PIP processor only during multi-channel mode (FF-SPIP only). The inversion of FXTAL at the collector of Q8410 is used by the Encoder IC to reconstruct the 3.58 MHz portion of the chroma signal in the output stage.

During Multi-Channel mode, the Free Run 3.58 line goes high to disable the Big Pix chroma signal at U8401-1 and allows the 3.58 MHz oscillator to free run. The PIP Processor is instructed by the SPIP control micro U8901 over the PIP clock, data, and enable lines to use the FXTAL signal as a reference for the 20 MHz VCO instead of the unstable sync signal available during Multi-Channel mode. If the FXTAL signal is not present at the PIP processor, all PIP functions will operate normally but Multi-Channel mode will produce a picture with horizontal tearing.

Video Inputs

Big Pix Chroma
The Big Pix chroma signal is used as a reference by the PIP processor to establish the chroma level of the small pix. The big pix chroma signal is amplified by Q8505 and applied to the voltage to current converter Q8506. The chroma signal at the emitter of Q8505 is gated by the burst gate signal from the sync separator Q8411, 12 in D-SPIP and by the composite sync out of U8501-47 in the FF-SPIP modules.

Q8506 creates a current into pin 7 of U8501 which is proportional to the amplitude of the big pix chroma burst. The pip processor matches the small pix chroma to the level of the big pix by using this reference current. Although pin 7 is a current input, the voltage at this pin varies between 3 to 4 VDC depending upon the level of the big pix chroma burst. As the big pix chroma level decreases, the voltage at pin 7 increases to produce less chroma in the small pix. The reverse is true when the big pix chroma level increases.

If there is no chroma burst in the big pix, the voltage at pin 7 goes to about 4 VDC and produces no chroma in the small pix even though the source for the small pix may contain chroma information. This is the case where a loss of chroma in the small pix appears to be a color killer problem in the Decoder U8301 when actually the loss is caused by no chroma in the big pix. If you check the R-Y/B-Y inputs to U8501, you will find signals are present indicating that the color killer from the decoder is not activated.

During full field special effects (FF-SPIP only), there is no need to match big and small pix chroma since the small pix is not activated. The big pix chroma reference is removed from Q8505 by Q8507. During full field effects such as freeze or zoom, the fast switch line at the base of Q8507 stays high. This turns on Q8507 to disable the big pix chroma from entering the reference circuit. When the small pix is enabled, the fast switch line pulses high but does not turn Q8507 on due to the RC time constant in the base of Q8507. In actuality, Q8507 does conduct somewhat to slightly decrease the chroma signal at Q8505, but not enough to affect circuit operation.

Y, R-Y/B-Y
The insert (PIP) luma signal is applied to the PIP Processor at pin 12. The R-Y and B-Y signals from the decoder stage enter the PIP processor at pins 14 and 16. All three signals are digitized by the pip processor and stored in the VRAM. The Y REF adjustment R8517 at pin 8 sets the output level of the small pix luma signal.

VRAM (Video Ram)
The PIP Processor converts the incoming analog video information into digital data. Once converted, two fields of digitized video data are stored in the VRAM U8502. Data is transferred *to* the VRAM through pins 10, 11, 8, and 7 of U8502 and read *from* VRAM through pins 17, 16, 1, and 2.

A 20 MHz clock produced in the PIP Processor is supplied to the VRAM pin 5. The clock is needed for timing within the VRAM IC. Without this clock, all PIP functions are disabled.

There are six control pins on the PIP Processor which control Data to and from the VRAM:

TAS - Transfer Address Strobe
SAS - Serial Address Strobe
SAD - Serial Address Data
WE - Write Enable
CGW - Clock Gate Write
CGR - Clock Gate Read

Although the timing on all these control lines would be nearly impossible to decode with common service equipment, the following list gives some quick logic checks for verifying VRAM operation.

Troubleshooting Tip

Signal	*PIP Off*	*PIP On*
TAS	Inactive	Low going Pulse
SAS	Inactive	Low going Pulse
SAD	Inactive	High going Pulse
WE	Inactive	High going Pulse
CGW	Inactive	Low going Pulse
CGR	Inactive	High going Pulse

The write enable (WE) line is a good starting point when troubleshooting the VRAM. When the small pix is turned off, the WE line is high. With the small pix turned on, the WE line should pulse high to signify that the PIP processor U8501 is attempting to write and read data from the VRAM. If this signal is not present, small pix video information may appear outside of the small pix border.

Data In and Out lines except for Data Out bit 1 (U8501-30) are inactive when the small pix is turned off and active when small pix is turned on. With the small pix on, the Data Out lines of U8501 contain continuous square wave activity. When the small pix is turned on, the Data In lines of U8501 are inactive during the vertical sync interval of the big pix. This can be viewed on a scope when troubleshooting.

A defective data line will produce distorted or mosaic video effects in the small pix or frozen big pix. The amount of distortion is dependent upon which data line is defective. If all data lines are defective, no PIP functions will operate.

Defective control lines (TAS, SAS, WE, etc.) produce noise glitches outside of the small pix border.

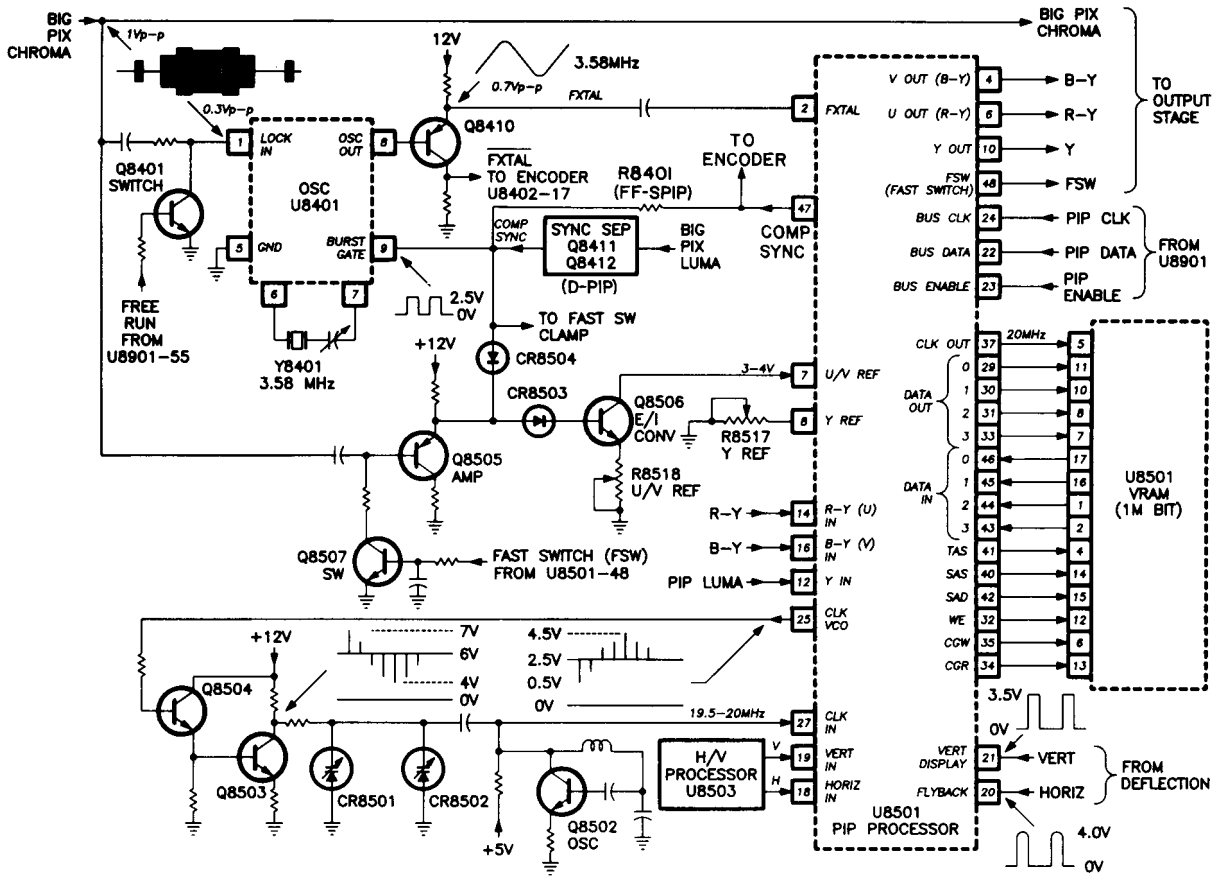


Fig. 39 SPIP Processor (repeated)

Control Signals

All operational commands are transmitted to the PIP Processor from the SPIP control micro U8901 through the PIP Clock, Data, and Enable Lines at U8501-24,22,23. As mentioned earlier, the SPIP control micro receives its operation commands from the system control micro U3101 on the main chassis.

Troubleshooting Tip

When diagnosing a PIP problem, check for activity on the PIP clock, PIP Data, and PIP Enable lines. With the small pix turned off, all lines should be high with no activity. When you turn the small Pix on, all lines should pulse low every 80 milliseconds. Move the time base on your scope to approximately 0.2 msec/divison to see if the lines are swinging from 0 to 5 VDC. If data is not present on these lines, troubleshoot the key signals going to U8901. Loss of vertical reset at pin 16 of U8901 will cause U8901 to never activate the PIP clock, data, and enable lines.

Output Signals

The digitized video data from the VRAM is read back into the PIP processor and converted back to analog signals. The analog video outputs from the PIP processor containing the small pix or special effects video information are B-Y, R-Y, Y, and Composite Sync at U8501-4,6,10, and 47. The Fast Switch signal at pin 48 is used by the Output stage to select between big and small pix information. These signals are used by the output stage which will be discussed in the next section of this manual.

PIP Processor Troubleshooting

Symptom: No small Pix chroma.

1. Make sure big pix contains chroma burst, if not, small pix will be monochrome. Check for 3.58 MHz from U8401. Verify color reference at U8501-7. Make sure decoder stage is providing R-Y/B-Y signals to U8501.

Symptom: Small pix chroma is not sync locked, floats through picture.

1. Verify burst gate pulse at U8401-9.
2. Check burst gate position at decoder U8301-1 in previous section.

Symptom: No PIP features.

1. Check for activity on PIP clock, data, and enable lines on U8501 according to explanation given in this section.
2. Check for 20 MHz VCO and VRAM operation as described in this section.

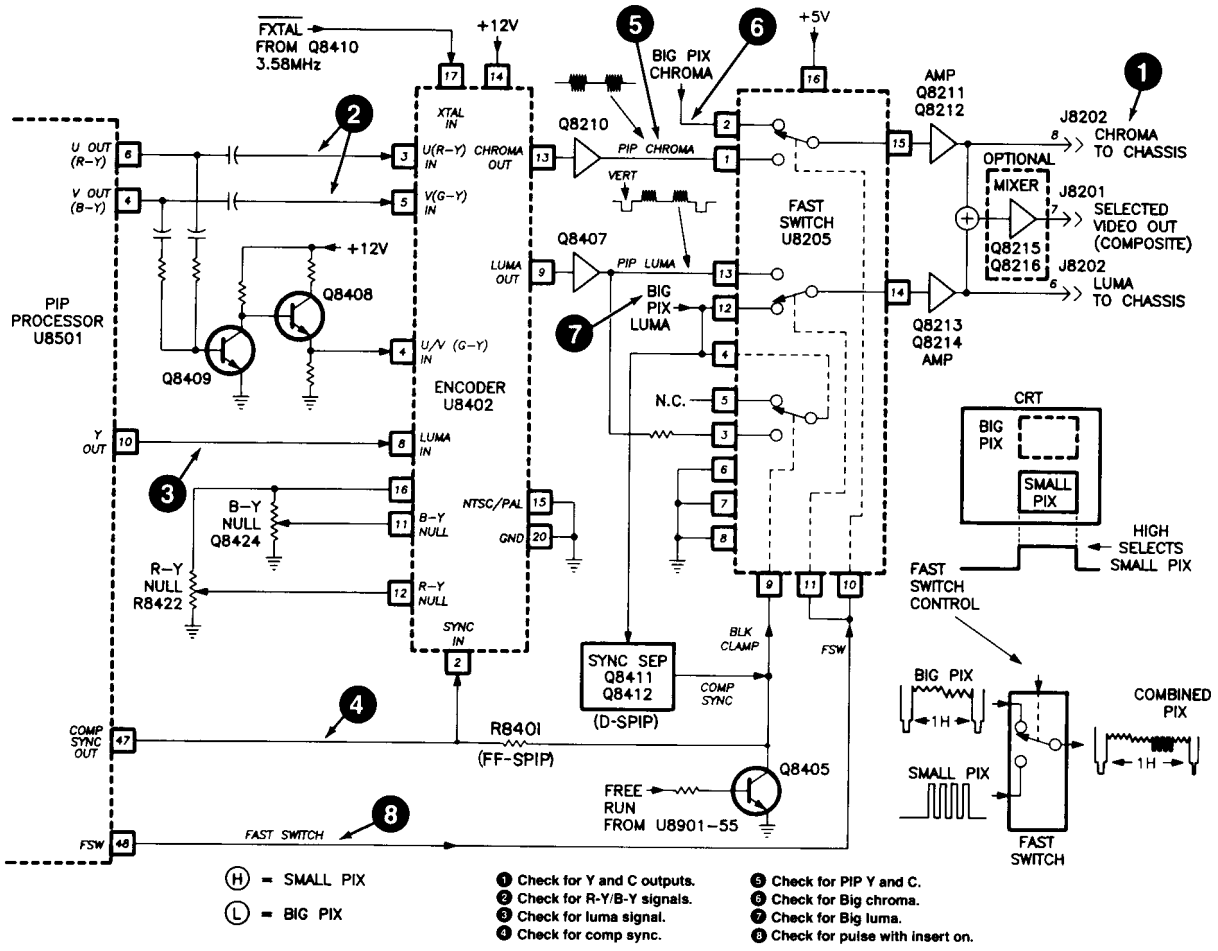


Fig. 40 Encoder and Output Stage (SPIP)

Symptom: Small pix rolls vertically through the big pix or tears horizontally across big pix.

1. Check H and V inputs to pins 18, 19, 20, and 21 of U8501.

Encoder and Output Stage

Purpose of circuit:

1. Convert PIP R-Y/B-Y to 3.58 MHz chroma signal and insert composite sync into PIP luma signal.
2. Fast Switch (mix) small pix information into big pix video signal to create big and small pix on the screen.
3. Clamp the black levels of the big and small pix to the same level.

Encoder

The small pix color output of the PIP processor U8501 is in R-Y and B-Y format. These signals must be converted to the standard 3.58 MHz chroma signal before being applied to the chassis. This is the purpose of Decoder U8402. The R-Y and B-Y signals are matrixed by Q8409 and Q8408 to create the G-Y signal. All three signals enter the decoder IC at pins 5, 4, and 3.

The 3.58 MHz FXTAL (bar) signal enters U8402 at pin 17 to recreate the 3.58 MHz portion of the chroma signal. The R-Y and B-Y Null adjustments are used to obtain the proper levels of R-Y and B-Y to match the small pix color temperature with the big pix color temperature.

The Luma signal from the PIP Processor U8501 does not contain composite sync. Composite sync at U8402-2 is added to the luma signal within the encoder IC.

The output signals of the Encoder are PIP Chroma and Luma. The waveforms shown after Q8210 and Q8407 show one vertical field of the PIP luma and chroma signals. Notice that there are two occurrences of luma and chroma which represent two small pix inserts. The PIP processor reads the PIP insert two times during one field. The fast switch ensures that one one of these bursts reaches the screen. The diagram in the middle right sec-

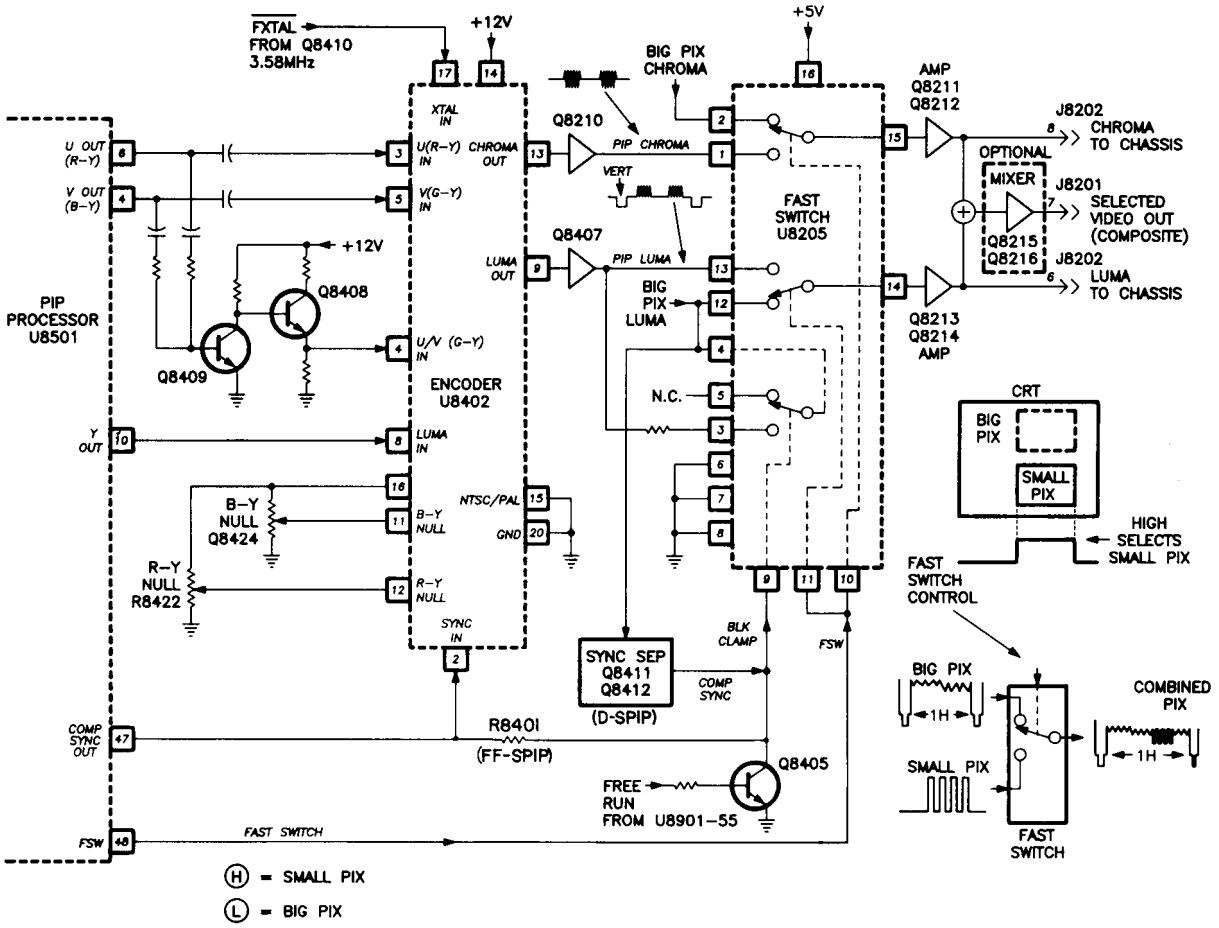


Fig. 40 Encoder and Output Stage (SPIP) (repeated)

tion of figure 40 shows the small pix displayed on the CRT. If it were not for the fast switch, the dashed box representing another small pix would also be viewable.

Fast Switch

Now that the small pix signal is converted to luma and chroma signals, they must be mixed with the big pix luma and chroma signals to produce the picture on the screen.

The Fast Switch U8208 selects either Big Pix Y/C signals or small pix Y/C signals. The Fast Switch (FSW) control line selects between the two. When PIP is off, the FSW line remains low to pass only Big Pix Y/C signals to the output. When PIP is turned on, the FSW line goes high at the appropriate time to switch the small pix Y/C signals to the output. Timing of the FSW is controlled by the PIP processor U8501 to pass only one of the two bursts of PIP luma and chroma information. During full field special effects such as Freeze or Zoom (FF-SPIP only), the FSW line stay high to pass the digitized picture to the screen.

The operation of the fast switch is shown in the lower right hand corner of figure 40. One input to the switch is one horizontal line of big pix chroma. The other input to the switch is the one horizontal line of PIP luma. At the appropriate time, the fast switch control line toggles the switch to the lower position to pass the small pix luma to the output. The result is one horizontal line of big pix information with the small pix luma inserted where needed.

Black Clamp

The back porch blanking level of the small pix must be clamped to the same level as that of the big pix. The black clamp operation is executed within U8205 by the switch connected to pins 3 and 4.

In D-SPIP modules, the big pix luma signal enters a sync separator consisting of Q8411 and Q8412. The sync output is applied to the switch control at pin 9. When the sync signal at U8205-9 goes high during the blanking interval, pins 3 and 4 are tied together by the internal switch. This connects the big pix luma signal to the small pix luma signal to clamp the small pix back porch to the level of the big pix back porch.

In FF-SPIP modules, R8401 is installed to supply the clamp pulse from the composite sync output of U8501 instead of from the sync separator Q8411, Q8412. The output of Q8411 and Q8412 is disabled in the FF-SPIP modules.

During multi channel mode, the free run control from the SPIP control micro U8901 goes high. The high turns on Q8405 to pull the clamp signal at U8205-9 low. This disables the black clamp circuit since the black level changes from one channel to the next during the multi channel mode.

Output Stage to Chassis
The luma and chroma signals from the fast switch are buffered before being applied to the chassis. The Y/C signals are applied to the Y/C inputs of the one chip.

In future SPIP modules, the luma and chroma signals may be combined to create a composite video output containing the big and small pix information which will be applied to selected video output jack on the back set. This will allow you to view the video signal containing the small pix and all video effects on an external monitor or to record the signal on a VCR.

Troubleshooting Tips

Symptom: Small pix color temp doesn't match big pix.
1. Try to adjust R-Y and B-Y Null controls. If match still cannot be made, check for R-Y, B-Y and G-Y inputs to Encoder U8402. If OK, check Burst Blank adjustment on Decoder U8301.

Symptom: No PIP features, normal viewing OK.
1. Check Fast switch signal. If always low, only big pix picture can be selected.

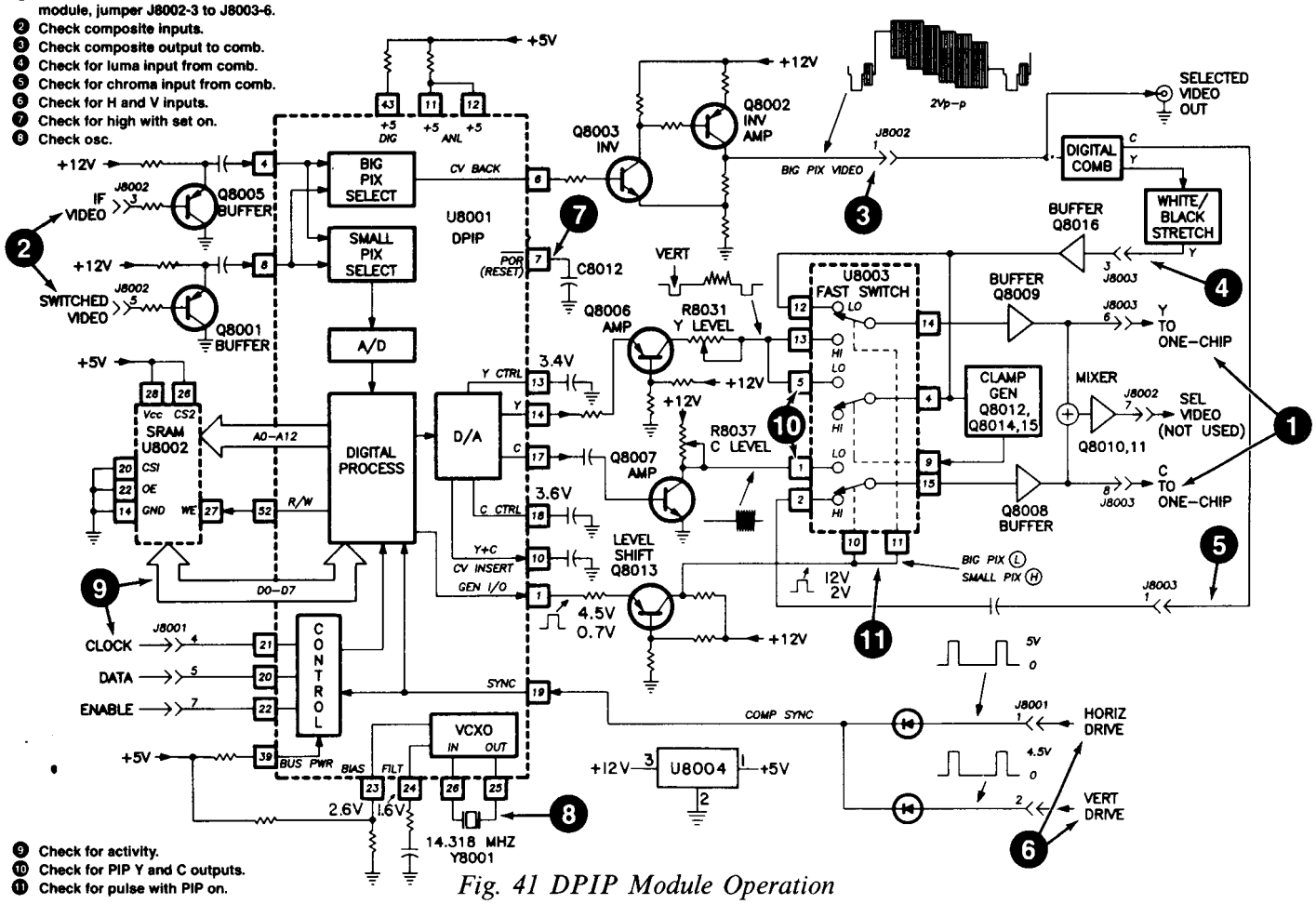


Fig. 41 DPIP Module Operation

Figure 41 shows the circuits contained in the DPIP module. As mentioned in the PIP operation guide in this manual, DPIP produces a small pix insert which can be frozen, moved, and swapped with the big pix. It contains no full field effects such as freeze, zoom, or multi-channel.

The DPIP module is much simpler than the SPIP module described earlier because much of the complexity has been integrated into the DPIP processor U8001. This makes troubleshooting this module much easier than the SPIP module since about all that is left to do is signal trace.

Composite Video Inputs/Outputs

Just as in SPIP, the DPIP module receives the composite TV tuner signal at J8002-3 and the switched video source from U1401 on the chassis. These signals are used as sources for the big and small picture content. However the source selection is contained within U8001 instead of switch ICs used in the SPIP module.

Big Pix Signal Path

The big pix video signal is selected within U8001 and exits the IC at the composite video back (CV Back) pin 6. The signal is inverted twice and amplified by Q8003 and Q8002 before it exits the DPIP module for application to the comb filter on the chassis and the selected video output jack on the back of the set.

The big pix Y and C signals from the comb enter the DPIP module at J8003 pins 3 and 1. The big pix luma signal is applied to the fast switch U8003 pins 4 and 12 and also to a clamp pulse generator stage. The big pix chroma signal is applied to the fast switch U8003-2. The function of the clamp and fast switch U8003 will be discussed later.

Small Pix Signal Path

The small pix video signal is also selected within U8001 like the big pix source selection, but the small pix source does not exit the IC. Instead, it enters the analog to digital converter stage to be converted to digital information for the PIP processor.

SRAM

The digitized small pix video data is stored in SRAM (Static Ram) U8002 and recalled when needed to produce the small pix information. Data is transferred to and from the SRAM over eight data lines D0 through D7. The storage location within the SRAM is selected by thirteen address lines A0 through A12. The write enable

line selects whether data is being read to or from the SRAM. These lines are active at all times regardless of whether the small pix is turned on or off.

Operational Commands
Operational commands enter the module over the clock, data, and enable lines from the system control micro U3101 on the chassis. There is no dedicated control micro between the module and the system control micro as in the SPIP module. Activity is present on these data lines as described in the system control section of this manual. Power to the bus control stage within U8001 is supplied at pin 39 from the 5 volt supply.

VCXO
The main oscillator for U8001 is a voltage controlled 14.318 MHz oscillator at pins 25 and 26. The VCO is locked to the sync signal of the big pix to lock the small pix to the big pix. The bias for the VCO at pin 23 operates at approximately 2.6 VDC while the VCO filter at pin 24 operates at about 1.6 VDC. If either voltage is missing, the insert cannot be produced on the screen.

Power ON Reset (POR)
The pip module receives its power from the 12 volt run supply from the chassis. The 12 volt supply is supplied to a three pin regulator U8004 to derive the 5 volt supply for the module. When the set is turned off, all power is removed from the DPIP module.

When the set is first turned on, power has to established in the PIP module from the 12 volt run supply. After the 12 volt supply rises, the 5 volt supply from U8004 is established. U8001 is held in reset at pin 7 until the charge on C8012 rises to 5 volts. Check for five volts at the reset pin 7 when the set is on.

Sync Inputs
The DPIP module must receive horizontal and vertical pulses from the chassis to time the writing of the small pix into the big pix. The horizontal drive signal is summed with the vertical drive signal to produce the composite sync signal at pin 19 of U8001. If the horizontal portion of the composite signal is missing, the small pix cannot be turned on. If the vertical component is missing, the small pix rolls vertically through the big pix.

Y and C Outputs
U8001 produces the small pix Y and C signals at pins 14 and 17. The digitized small pix information is converted to analog information by the internal D/A. The bias control for the luma and chroma D/A is developed at pins 13 and 18. The level of the luma and chroma signals from U8001 is affected by the voltage at these pins. Normally the luma bias at pin 13 is about 3.4 VDC while the chroma control operates at about 3.6 VDC.

The Y+C CV Insert at pin 10 of U8001 is an optional composite video signal containing the small pix information. It is not used in this application.

The small pix Y and C signals from pins 14 and 17 are amplified by Q8006 and Q8007 before being applied to the fast switch U8003. The only adjustments in the module are the Y and C level adjustments R8031 and R8037. These controls adjust the amplitude of the small pix Y and C signals to match them to the levels of the big pix.

Notice that the waveforms showing the small pix Y and C signals in figure 41 contain only one burst of Y and C information in each field of video unlike the SPIP module which contained two. U8001 reads data from the VRAM only once per field instead of twice as in the SPIP module.

Fast Switch
The small pix Y and C signals are ready to be mixed or switched into the big pix. This is performed by U8003. This switch operates just as the fast switch in the SPIP module. The Y/C signals from the big pix are applied to pins 12 and 2 while the small pix Y/C signals are applied to 13 and 1.

The switches in U8003 pass either big pix Y/C or small pix Y/C to the output of the chassis, depending upon the logic level at pins 10 and 11 of U8001. When these pins are high, small pix information is passed and when low, big pix information is passed to the output. The control line for this switching originates from the GEN I/O line from pin 1 of U8001. The logic level swing at pin 1 is from 0.7 to about 4.5 VDC. This level is shifted by Q8013 to 2 - 12 VDC at pins 10 and 11 of U8003.

Clamp Generator
The small pix luma black level is clamped to the big pix black level by the middle switch in U8003. The clamp generator circuit consisting of Q8012, 14, and 15 removes sync from the big pix luma signal and applies it to the clamp switch control pin 9 of U8003. When the sync signal at pin 9 goes low, the switch in U8003 connects the small pix luma signal at pin 5 to the big pix luma signal at pin 4 to clamp them to the same black level.

The Y and C outputs for the fast switch containing the combined big and small pix information is buffered by Q8009 and Q8008 before being applied to the one-chip on the chassis. An optional mixer stage consisting of Q8010 and Q8011 may be used in the future to provide a composite video output containing both big and small pix information to the selected video output jack. Currently it is not being used.

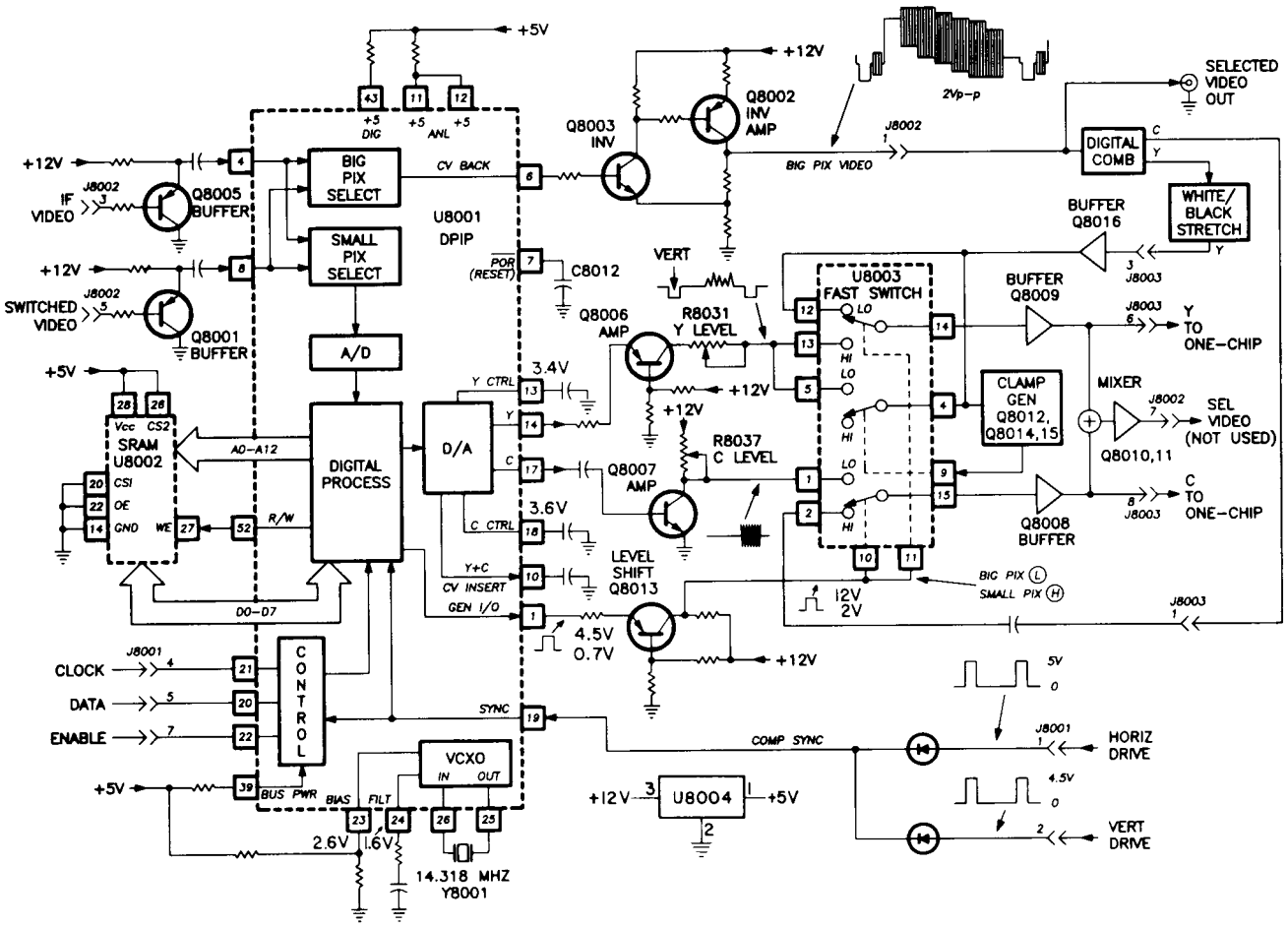


Fig. 41 DPIP Module Operation (repeated)

DPIP Troubleshooting

Just as with SPIP, the DPIP module may be bypassed by removing the module and jumpering the TV video source at J8002-3 to the Y and C inputs of the one-chip at J8003 pins 6 and 8. If this does not eliminate the problem, troubleshoot the chassis instead of the PIP module. If it does eliminate the problem, verify all signals going to and from the DPIP module before troubleshooting the module to the component level.

The easiest way to troubleshoot this module is to verify the signals mentioned in the previous circuit descriptions noting the symptoms given in some of the explanations.

Notes

CTC169 PROJECTION TELEVISION

Introduction

The CTC169 chassis is used in both direct view and projection television. There is little difference in the base chassis, however, the projection sets use a number of additional circuits to provide the proper signals to the three tubes. There are four models of projection receivers using the CTC169 chassis. Three models have a 46 inch screen and the fourth has a 52 inch screen. There are three RCA brand models (P46100, P46150, and P52150) and one GE brand model (46GW950).

All models have the following features:

- On-screen menu tuning and antenna selection
- TV/VCR/Cable remote control
- 181 channel tuner with auto programming and channel labeling
- Commercial skip
- Auto Demo mode
- Digital Comb Filter
- Dynamic Focus
- Black and White "Stretch" Circuits
- 13 I/O jacks including S-VHS connector and external speaker jacks
- 10 Watt per channel stereo amplifier with 2-2" tweeters and 2-5" woofers
- Digital stereo decoder system with expanded stereo and surround sound

In addition, the RCA P46150 and P52150 also have pix-in-pix.

There are a number of design changes which make these models unique. The mirror is made of mylar and is stretched over a frame. The mirror is hinged and is folded into the cabinet for shipping. This reduces the depth of the cabinet to allow it to pass through interior doors. Once the television is in position, the mirror must be pulled out to its fully extended position. Ten screws must be installed to hold the mirror in position.

The chassis, auxiliary circuit boards, picture tubes and lenses are mounted in a wooden frame. The entire kit weighs 68 pounds. The kit can be removed from the cabinet for servicing. The front panel assembly should also be removed since it is easier to remove the front panel assembly than it is to reach the connector to unplug the assembly.

The screen is removed along with the frame surrounding the screen. There are two spring clips located at the top of the frame that hold the screen in place. The screen must be removed to remove the front panel assembly. The spring clips are released by pressing a flat object against the spring in between the top of the cabinet and the frame around the screen.

The picture tubes come with the first lens assembly and are optically aligned. The tube comes with the anode lead glued to the tube. The other end of the anode lead fits into a spring loaded connector on the high voltage splitter assembly. The tubes are the same as the current projection sets, but the lens assembly is different. The tubes are liquid cooled, and no refill kit is available.

The customer convergence controls are located on the remote transmitter. When the convergence option is selected from the video menu, a small cross-hatch pattern appears in the center of the screen. The volume up and down controls are used to move the red and blue rasters so they are on top of the green. The service convergence controls are located at the bottom front of the television. The speaker grill cover is removed to gain access to the convergence controls. The controls are labeled with the order in which they are adjusted and a picture showing the effect the adjustment has on the raster. The convergence control panel can be removed to gain access to the front of the chassis and auxiliary board.

Chassis Familiarization

Rear projection television receivers differ from conventional television receivers in that three projection CRTs are used versus one direct-view CRT. Because projection televisions use three separate CRTs, the circuit areas can be divided into two categories. First are those circuit areas that are common to both direct view and projection receivers, such as tuner, IF, system control, and audio. Second are the circuit areas that are required for projection television receivers only, such as convergence generators and high voltage splitters.

The following circuit areas are common to both direct-view and projection television receivers:

- Tuner
- IF
- U1001 CTV Processor for video, audio, and deflection
- Digital stereo decoder
- 10 Watt per channel audio amplifier
- Digital Comb Filter
- Switching Regulator for both standby and run B+ supplies
- High voltage transformer
- System Control Microcomputer
- Front Panel Assembly with remote preamplifier

The circuits that are unique to projection televisions are located on various circuit boards in the instrument. The PTV AUX board is almost as big as the main chassis. The AUX board contains a switching power supply to provide power to the convergence circuits. six convergence power amplifiers, scan loss detector circuit, dynamic focus circuit, convergence signal generators, deflection yoke splitter, and video drive three way splitter. The convergence generator board generates the waveforms for the convergence amplifiers and contains the four D/A converters for the customer convergence controls. The high-voltage splitter provides a three way split of high voltage for the CRTs, a high voltage source for focus and screen, and buffered feedback for the high voltage regulator. The focus/screen module contains the red, green, and blue focus and screen adjustments and an adder for the dynamic focus signal. The CRT driver boards contain the red, green, and blue upper cascode video amplifiers and the scan loss beam cutoff circuit.

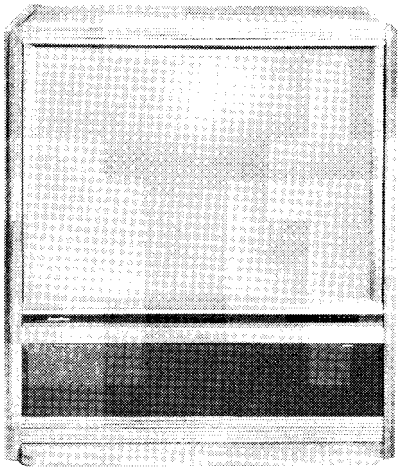


Fig. 42 RCA P52150 (CTC169 Chassis)

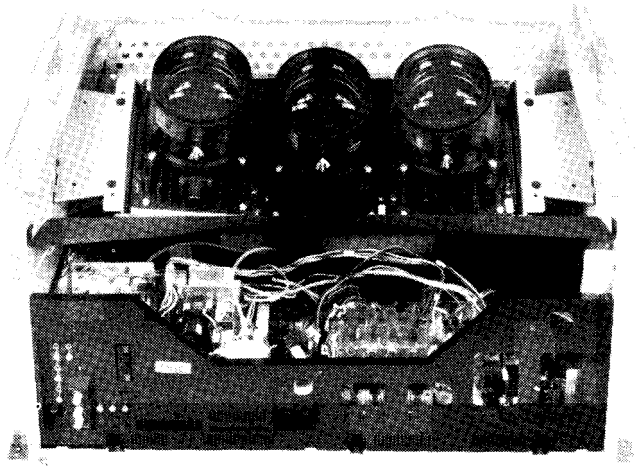


Fig. 43 CTC169 Chassis PTV Kit

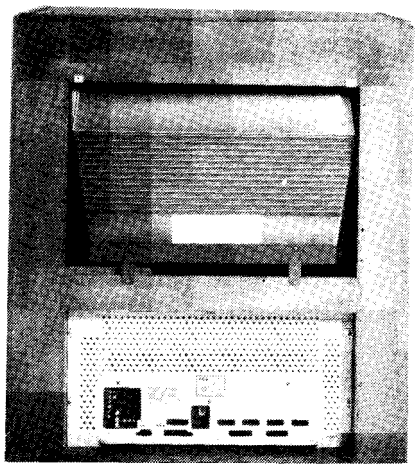


Fig. 44 Mirror in Shipping Position

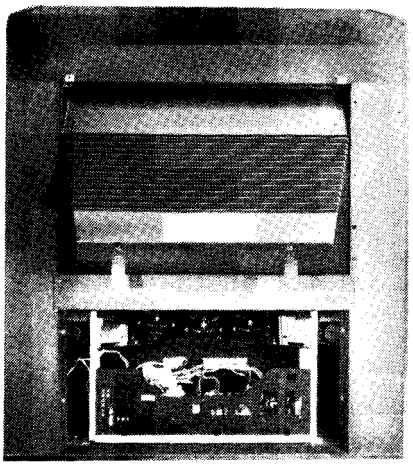


Fig. 45 Mirror in Viewing Position (Back Cover Removed)

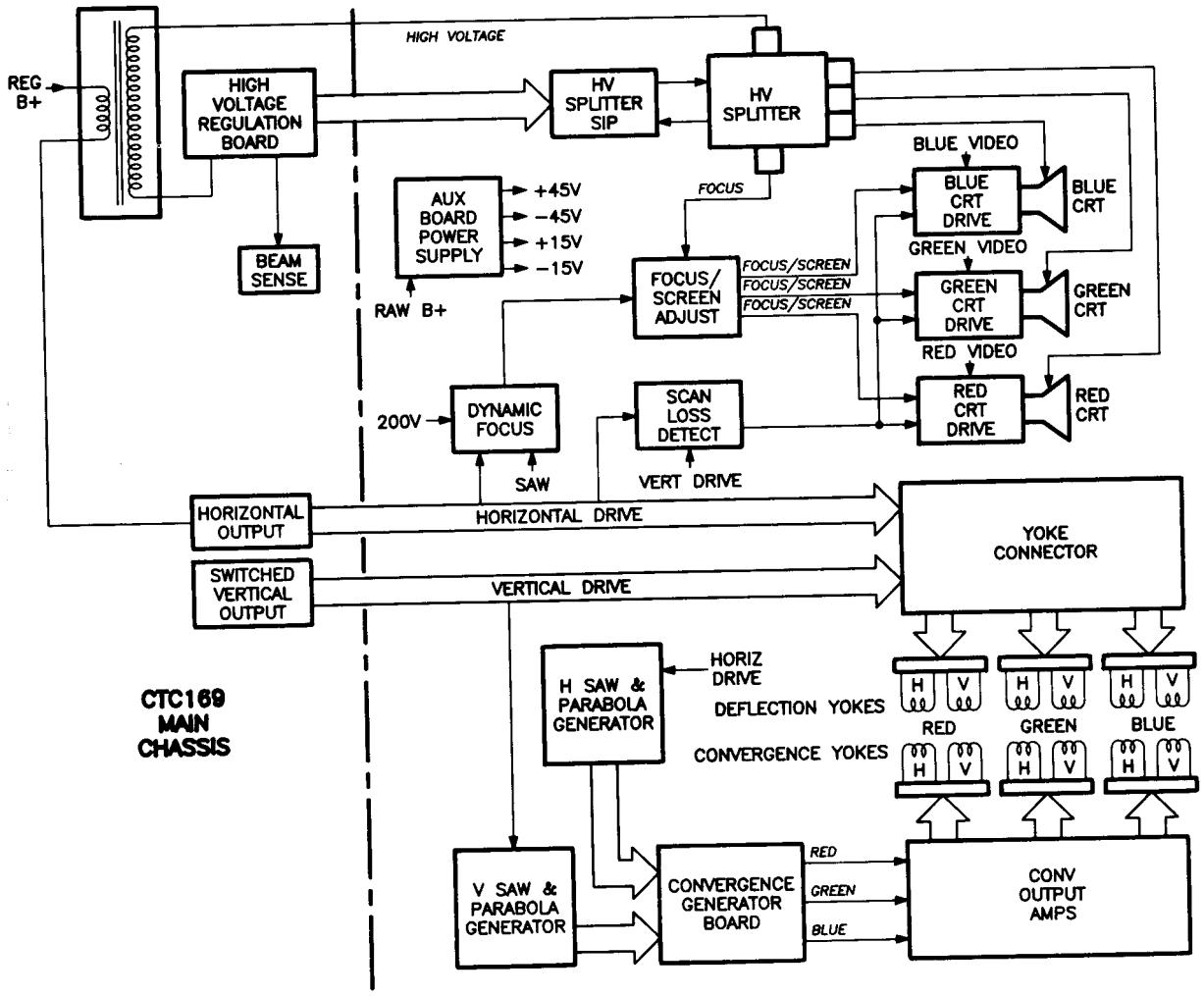


Fig. 46 Projection Block Diagram

The major difference between projection television and direct view receivers is the way the picture is sent to the screen. In direct view receivers, the picture tube has three guns, each of which is used to illuminate one color of phosphor stripes on the face of the picture tube. The picture is viewed directly on the face of the picture tube. In projection television, three picture tubes are used. Each tube has only one color phosphor on its face. The light from each tube is focused on a mirror and then reflected to a screen.

As three tubes are used, the convergence circuits are needed to make all three rasters the same size and shape. In direct view receivers, all three guns are close together, and one yoke can be made to converge the picture on the face of the tube. In a projection set, the tubes are all mounted at different angles, further complicating the convergence process.

In order to drive a projection television, certain outputs from the CTC169 chassis are routed to the PTV aux board. The high voltage output from the high voltage transformer is routed to a splitter. The splitter has taps to route the high voltage supply to the anode of each of the CRTs. In addition, the high voltage splitter also has a tap for the focus and screen controls. Each CRT requires a separate screen and focus control voltage. Because of the size of the screen used in the projection receivers, any raster distortion is more apparent than on a direct view set. A separate high voltage regulator circuit is employed to reduce any changes in the size of the raster due to changes in the high voltage supply. If the regulator was not used, the raster size could change with changes in the beam current. The high voltage regulator adds a voltage to the low side of the high voltage winding. Due to the multiplication factor of the winding, the anode voltage can be varied over a much greater range.

The projection television chassis also uses a dynamic focus circuit. The dynamic focus circuit modulates the focus voltage as the beam scans across the face of the CRT. In the center of the screen, the beam is focused in a small spot. In the corner of the screen, the spot tends to be stretched horizontally. The dynamic focus circuit changes the focus voltage to keep the spot size and shape constant.

The CRTs used in the projection set are small compared to the screen size. The tubes are driven at high beam current to obtain a bright picture on the screen. If for some reason either horizontal or vertical deflection stops, it is easy to burn the phosphor on the face of the tube. To prevent damage to the tubes, a scan loss protection circuit monitors both horizontal and vertical scan. If either scan stops, the scan loss protection circuit cuts off the tubes to prevent damage.

The horizontal and vertical drive signals from the main chassis are routed to the deflection yokes of the three CRTs. The horizontal yokes are connected in parallel and the vertical yokes are connected in series. These yokes serve the same function as in direct view receivers, they deflect the electron beam so that the beam scans across the face of the tube.

In addition to the deflection yokes, convergence yokes are used to cause all three rasters to have the same size and shape on the screen. Different correction signals are needed for each of the CRTs since the tubes are mounted at different angles. The green image is projected from the center CRT/lens assembly and is subject to less distortion than the red and blue images which are projected from the sides. The blue image is projected from the left side as viewed from the front of the screen. The distance from the blue lens to the left side of the screen is less than the distance from the blue lens to the right side of the screen. If the blue raster is the same size and shape as the green raster, the projected image will be keystone shaped. This occurs because the image spreads out as it is projected. Because the left side of the screen is closer to the lens than the right side, the left side of the image is smaller than the right side. The opposite effect is occurs to the red image which is projected from he right side of the screen.

To counteract the projection distortions, the rasters are intentionally distorted before they are projected so the resulting image has the proper geometry and convergence. The corrective raster distortions are generated by the convergence circuits and result in rasters that have the opposite distortion than the projected image. When the raster with the corrective distortion is projected, the distortions cancel resulting in a properly converged and shaped image in all three colors.

The convergence correction signals are developed by convergence generator. The inputs to the convergence generator are developed from the horizontal and vertical drive signals. The inputs are both vertical and horizontal sawtooth and parabola signals. These signals are combined in the convergence generator to provide the proper correction signal to the convergence output amplifiers. The convergence output amplifiers shift the level of the correction signals from the convergence generator to the proper level to drive the convergence yokes.

A separate switching power supply is used to provide power to the circuits unique to projection television. The regulator provides positive and negative 15-volt and 45-volt outputs. The regulator is configured much like the switching regulator used in the CTC149 chassis. In the CTC149, the switching regulator provided power to the audio output amplifier.

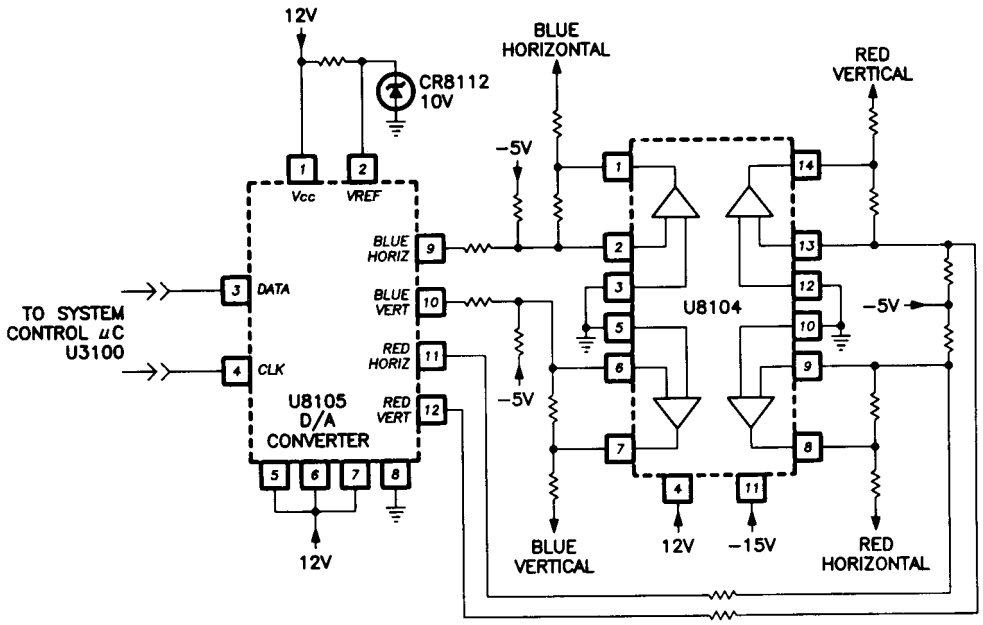


Fig. 47 Static Convergence Circuit

Static Convergence Circuit Operation

The static convergence circuit enables the customer to move the red and blue rasters with respect to the green raster. The green raster cannot be changed with the customer controls. The static convergence circuit provides a DC offset to the convergence generator circuit. By changing the DC offset, the entire raster is moved the same amount in the same direction.

When the customer convergence option is selected from the video menu, a small cross hatch pattern is displayed in the center of the video. This pattern is controlled by the system control microcomputer and is generated by the on-screen display IC. The instructions on the screen prompt the customer to adjust red and blue horizontal and vertical to place the red and blue rasters over the green.

When the customer convergence option is selected from the video menu, the crosshatch appears at the center of the screen. The color and direction of the adjustment are indicated by colored arrows that appear below the crosshatch. For example, the red horizontal adjustment is indicated by red arrows pointing left and right. The volume controls are used to change the convergence setting. After the red horizontal adjustment is completed, the + button is used to shift to the red vertical adjustment. Pressing + again shifts to the blue horizontal adjustment. When all of the customer convergence settings are completed, pressing the TV button returns the set to normal operation. The customer convergence settings are stored in the EEPROM and remain even after an extended loss of AC power.

The static convergence circuit consists of a digital to analog converter and a quad op amp IC. The D/A converter receives commands from the system control microcomputer. The microcomputer sends both the clock and data inputs to U8105. The digital to analog converter takes the data from the microcomputer and converts it to a DC level. The output of D/A varies between ground and 10 volts. The convergence generator requires both positive and negative voltages in order to move the raster in two directions. U8104 converts the output of the D/A to a level that can go above and below ground.

The D/A converter uses a reference voltage developed by CR8112. The 10 volt input is divided into 64 steps. The output of the D/A can vary between 0 and 10 volts in 64 steps. The output of the op amps to the convergence generator varies depending on the feedback resistor. All can vary at least 1.5 volts above and below ground. The red vertical output can vary approximately 3.4 volts above and below ground.

Malfunctions in the static convergence circuit will cause the entire raster to be shifted in one direction. To confirm operation of the D/A converter, monitor the output of the D/A and vary the corresponding input control. The voltage at the output should change from 0 to 10 volts. If the voltage does not change, check for activity on the clock and data inputs from the system control microcomputer. If the inputs are present, suspect a defective U8105. If the output range is incorrect, suspect a leaky CR8112. If the output is correct, check for a varying DC voltage at the output of U8104. The signal should vary above and below ground. If the voltage range is incorrect, suspect a problem in the feedback resistor or bias supply. If the output is at either of the supply voltages (12V or -15V), suspect a defective U8104.

Vertical Sawtooth and Parabola Generator Operation

The vertical sawtooth and parabola generator circuit develops two of the correction signals for the convergence generator circuit. The correction signals are combined in various ways with the horizontal rate sawtooth and parabola waveforms before the corrections are applied to the convergence yokes. The waveforms are combined in the modulator circuits.

The vertical reset pulse from the CTV processing IC U1001 is applied to the base of sawtooth generator Q8121. The positive pulse causes Q8121 to turn on. When Q8121 is on, the capacitor in the base of Q8123 is discharged. When the reset pulse goes Lo, the capacitor begins to charge. The charging current is supplied from Q8122. Q8122 is a constant current source, providing a constant charge current to the sawtooth capacitor.

The sawtooth waveform is buffered by Q8123 and routed to both another buffer and an operational amplifier. Q8120 routes the sawtooth waveform to the modulator circuits. The operational amplifier is used as an integrator. The sawtooth input is integrated to form the parabola output. The capacitor connected from the output at pin 7 to the input at pin 6 of U8107 causes U8107 to act as an integrator. Q8138 is turned on when the vertical reset pulse goes Hi at the start of vertical retrace. The transistor is used to quickly discharge the integrator capacitor during retrace. This is done to make sure that the parabola has the same amplitude and no DC offset. The output of the integrator is routed to the modulator circuits where the parabola is combined with horizontal rate correction signals.

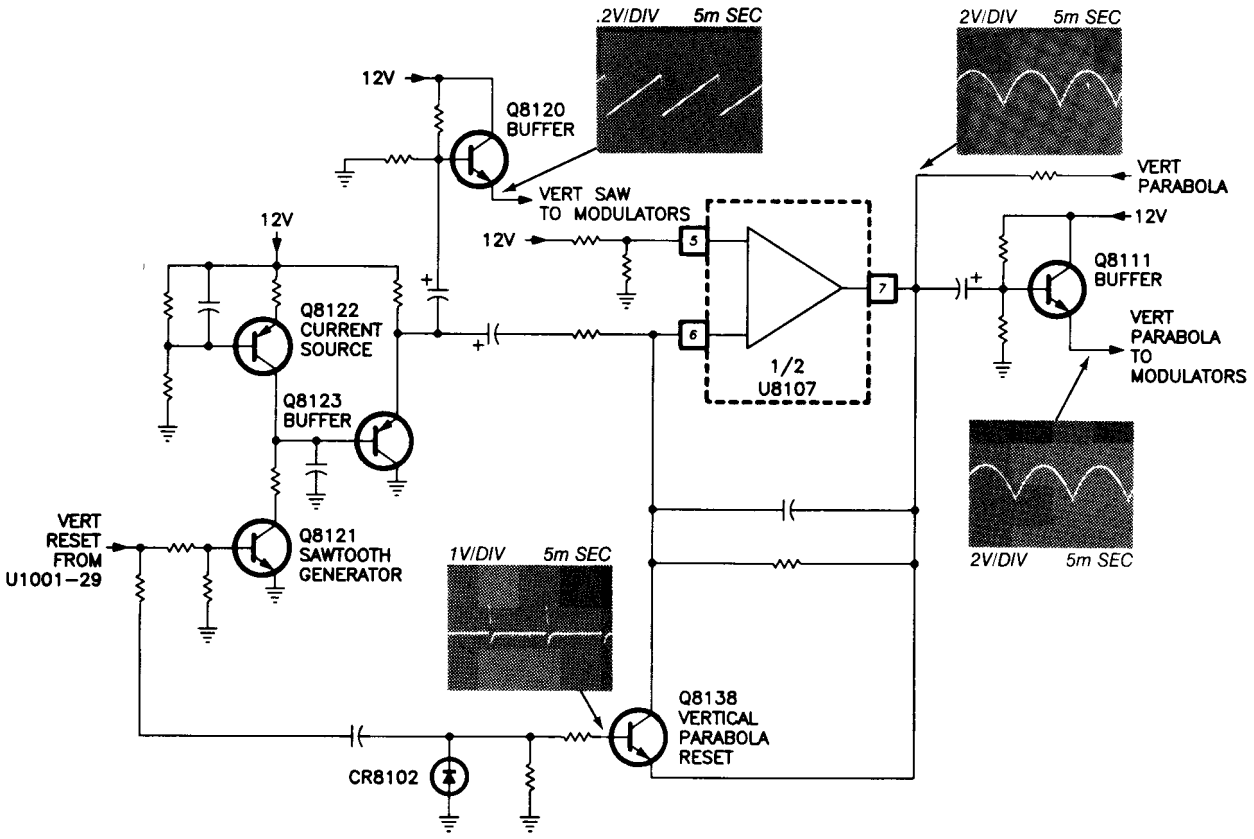


Fig. 48 Vertical Sawtooth and Parabola Generator

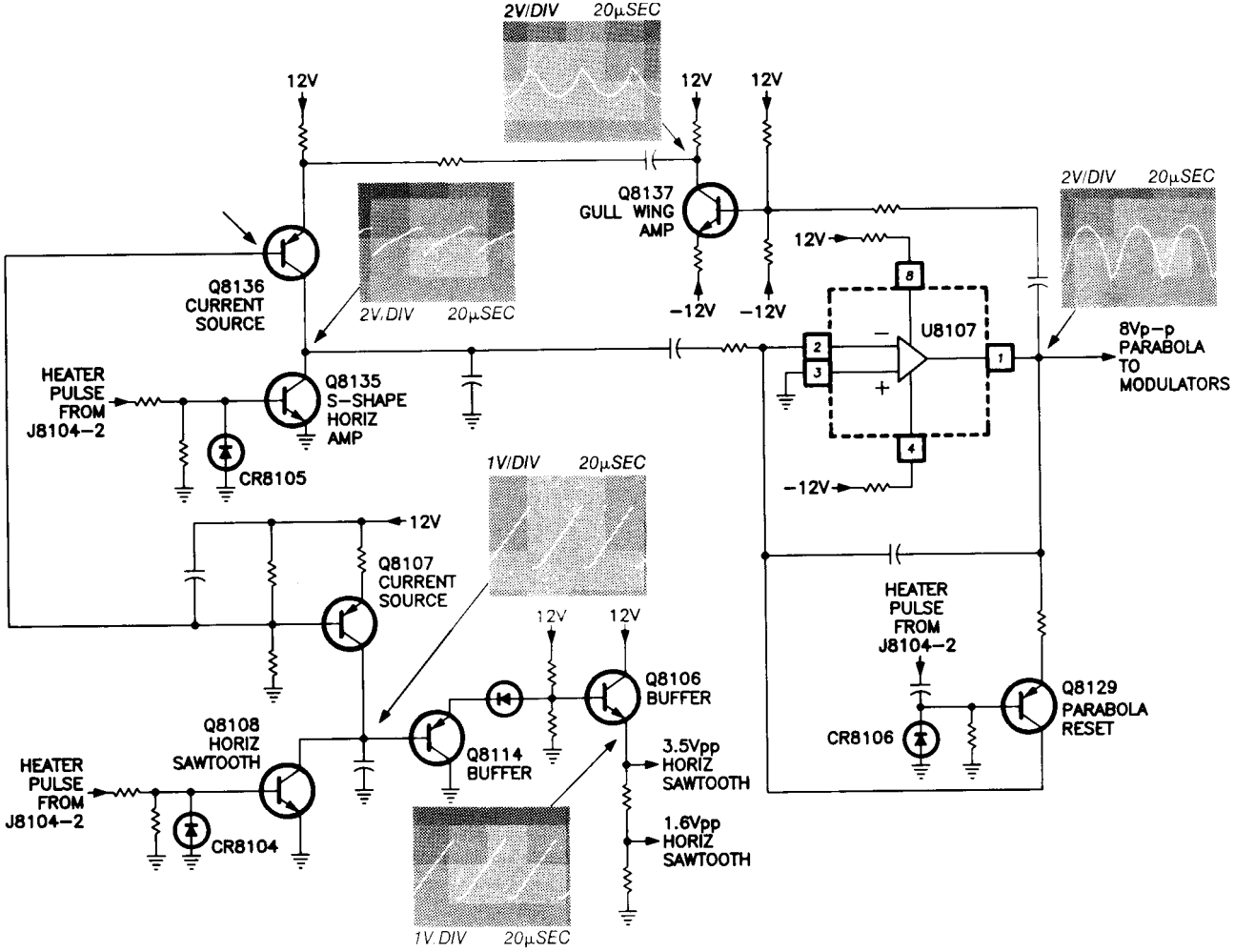


Fig. 49 Horizontal Sawtooth and Parabola Generator

Horizontal Sawtooth and Parabola Generator Operation

The operation of the horizontal sawtooth generator is very similar to the vertical sawtooth generator. The horizontal circuit is slightly different since two sawtooth generators are used. The first provides a sawtooth output for the modulators. The second sawtooth is combined with the parabola waveform to provide a slightly different input to the parabola circuit.

The two constant current sources, Q8136 and Q8107, share the base biasing resistors. The capacitor at the base of Q8114 develops the sawtooth waveform. The heater pulses from the high voltage transformer turn Q8108 on during horizontal retrace. When Q8108 is on, the sawtooth capacitor is discharged. The sawtooth is routed through buffer Q8114 to the base of Q8106. The diode at the emitter of Q8106 limits the waveform to keep the base of Q8106 above ground potential. The sawtooth waveform is routed through buffer Q8106 to a resistor voltage divider. Two horizontal rate sawtooth waveforms are routed to the modulators.

The second sawtooth waveform is developed by the capacitor at the collector of Q8135. This sawtooth is modified to have an "S" shaped correction voltage added to it. Again, the heater pulse from the high voltage transformer is used to reset the sawtooth capacitor. The charging current is supplied from Q8136. The sawtooth is coupled to an integrator to develop a parabola waveform for the modulator circuits. The capacitor connected from the output to the inverting input of the op amp develops the parabola. Q8129 discharges the parabola capacitor during horizontal retrace.

The gull wing or "S" shape correction is developed by feeding the parabola output back to the sawtooth input. This output is used with the vertical sawtooth waveform for vertical pincushion correction. The feedback is inverted by Q8137 and modifies the charging current for the sawtooth capacitor.

Convergence Modulators

The basic correction signals consist of the horizontal sawtooth and parabola and the vertical sawtooth and parabola. These signals are combined in the modulators to develop various inputs to the convergence circuits. A number of modulator circuits are used, but only a representative sample is shown in the manual. The operation of the modulators which are not covered is similar to the operation of the ones which are discussed.

The vertical parabola/horizontal sawtooth modulator provides an input to the red, green, and blue horizontal pin cushion correction circuits. The vertical parabola allows the correction signal to have a greater effect at the middle of vertical scan (the center of the screen) where the horizontal pin distortion is greatest. The correction signal has very little effect at the top and bottom of scan where the pin distortion is minimum.

The inputs to the modulator are the horizontal sawtooth and a vertical parabola. The inputs to the modulator have high impedance to minimize the interaction of the adjustments. R8193 is the vertical parabola preset adjustment and is adjusted to obtain a symmetrical output waveform. The parabola and sawtooth are combined in U8102 and the output signal is routed through a buffer to the pin cushion correction adjustments.

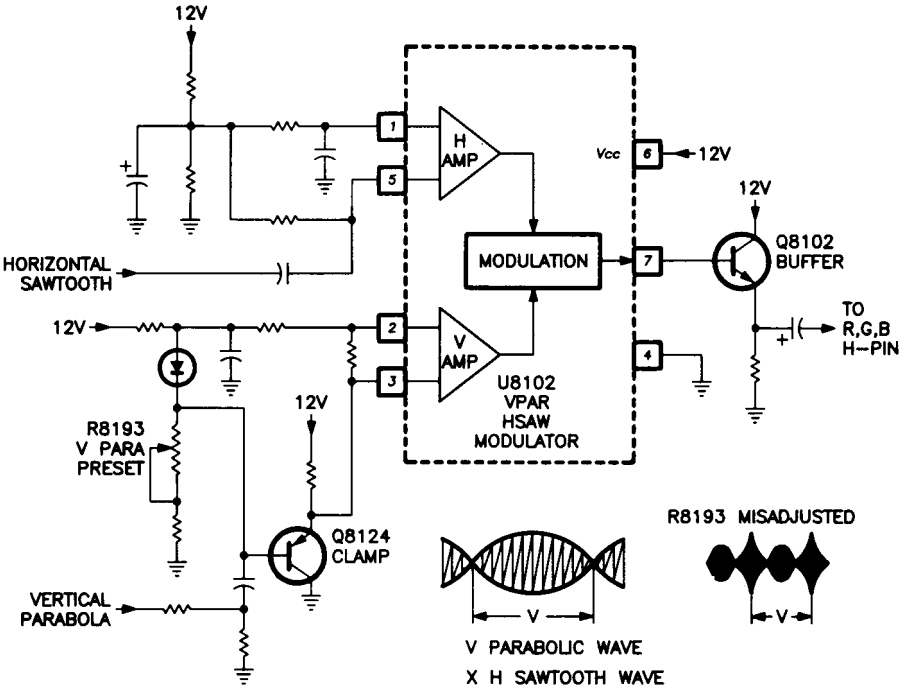


Fig. 50 Vertical Parabola/Horizontal Sawtooth Modulator

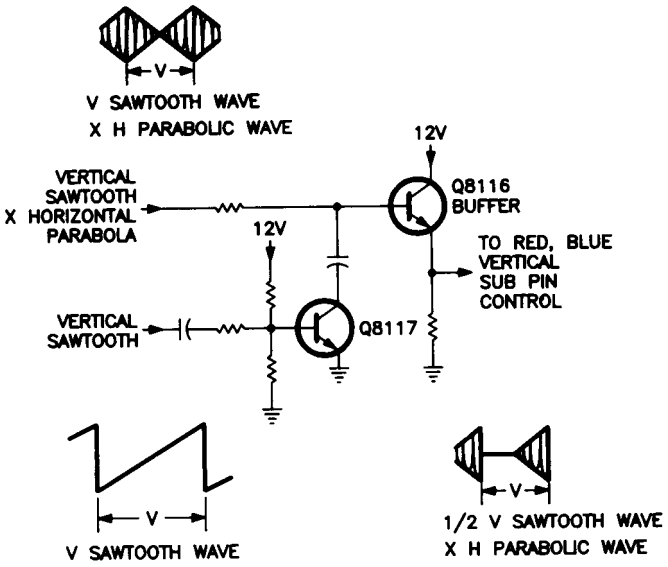


Fig. 51 Vertical Sub Pin Signal Generator

Certain corrections require different amounts of correction on different parts of the screen because of the way the tubes are mounted. For example, the horizontal pin cushion correction for the green tube is the same for both sides of the screen, but the red and blue rasters need different amounts of correction on either side. The horizontal sub pin signal generator provides a correction signal that affects only the left side of the raster. This circuit consists of a buffer and a clamp circuit. The vertical parabola/horizontal sawtooth is routed to both the buffer Q8113 and the clamp Q8112. The circuit passes only the bottom half of the vertical envelope. The resulting correction signal is routed to the red and blue horizontal sub pin adjustments.

Similarly, the red and blue tubes need different amounts of pin correction at the top and bottom of the screen. The vertical sub pin signal generator provides a signal which consists of half of the vertical sawtooth/horizontal parabola waveform. This signal affects only the bottom half of the raster.

The vertical sawtooth waveform is applied to the base of Q8117. The positive portion of the waveform turns Q8117 on. When Q8117 is on, the vertical sawtooth/horizontal parabola at the base of Q8116 is AC grounded. When the vertical sawtooth is below the point where Q8117 turns on, the correction signal is passed through buffer Q8116 to the red and blue sub pin controls.

Malfunctions in any of the modulators will appear as convergence problems on the screen. The service data contains waveforms and a drawing of the raster distortion corrected by each of the convergence signals. The use of this information should aid in quickly locating any defective components.

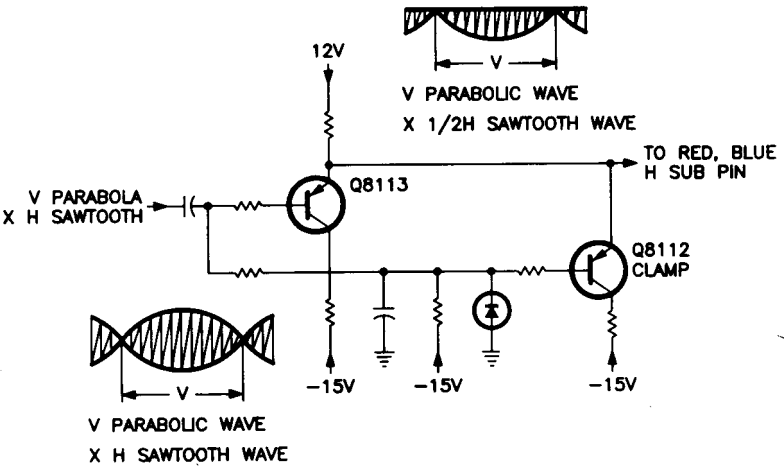


Fig. 52 Horizontal Sub Pin Signal Generator

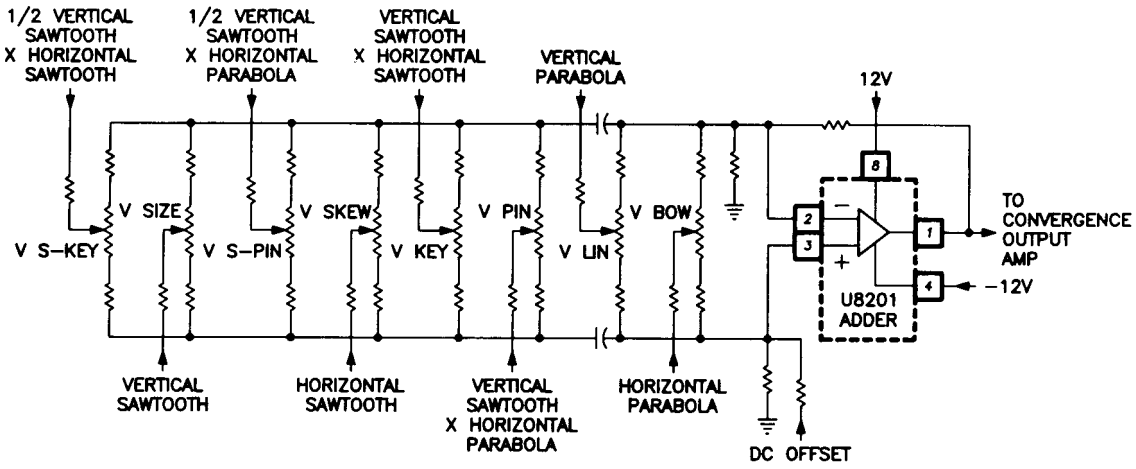


Fig. 53 Blue Vertical Convergence Circuit

Convergence Adjustment Circuit Operation

The convergence correction signals are combined at the convergence adjustment circuit and then routed to an output amplifier. The adjustment circuit combines all of the correction signals for one tube. There are separate adjustment circuits for the red, green, and blue horizontal and vertical signals. The green correction circuits have fewer inputs since the green raster requires less correction. However there is no difference in the circuit operation for either horizontal or vertical or for the particular color tube. The blue vertical convergence adjustment circuit is representative of the other five convergence adjustment circuits.

The blue vertical convergence adjustment circuit contains eight separate adjustments in addition to the customer or static convergence inputs. All of the convergence adjustments are located on the front of the unit, under the speaker grille cover. the control panel is labeled with the order in which the adjustment is made and a drawing which shows which portion of the screen and the type of correction for each of the controls.

The vertical convergence correction signals are routed to the wiper of the particular adjustment potentiometer. The potentiometer is part of a resistor divider network. The ends of the resistor divider are connected to the inverting and non inverting inputs of an operational amplifier. By moving the wiper in one direction, more of the correction signal is applied to the non inverting input, adding the correction in one direction. When the wiper is turned in the opposite direction, more of the signal is applied to the inverting input. This causes the correction signal to be in the opposite direction. Most of the correction signals are AC coupled to the adder to prevent interaction with the customer convergence controls. The DC offset voltage is developed by the static convergence circuit and are set by the customer convergence adjustments. The output of the adder is routed to the blue vertical convergence output amplifier.

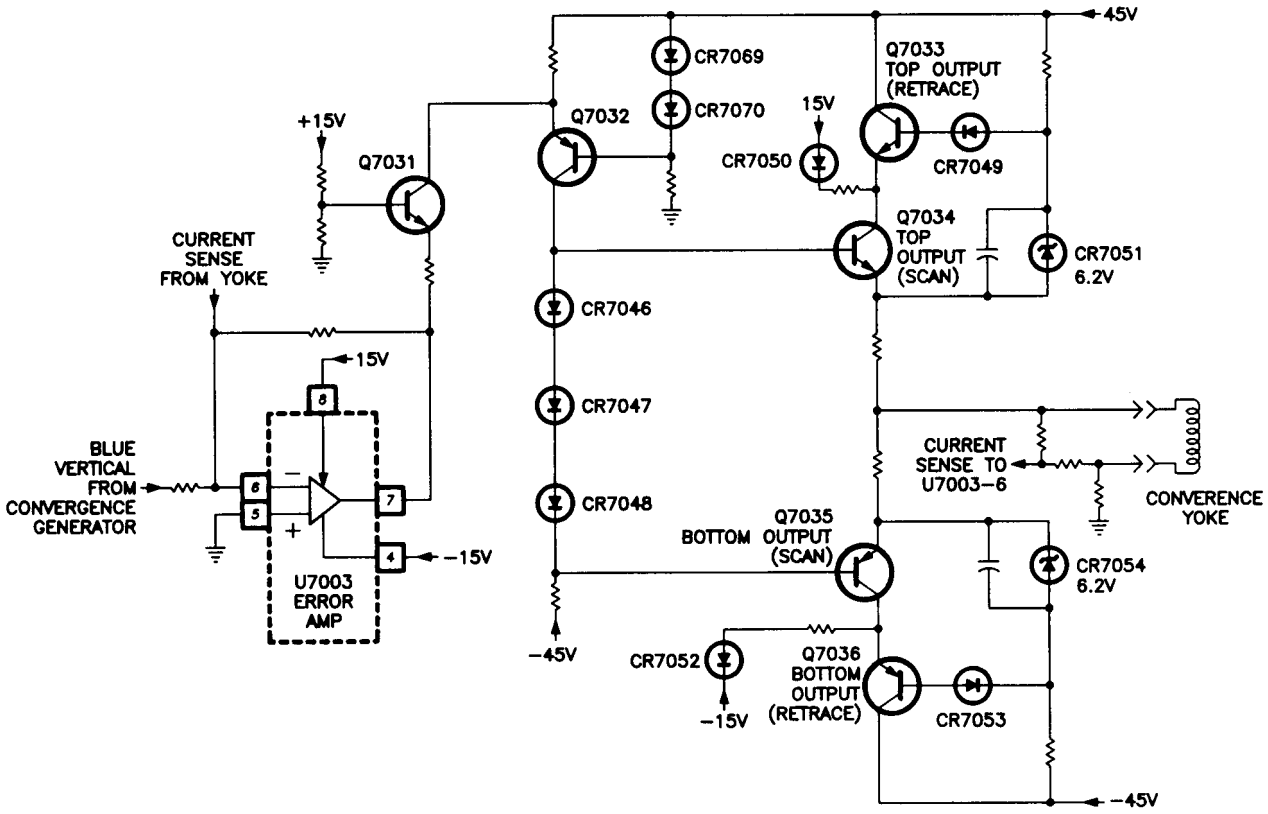


Fig. 54 Blue Vertical Convergence Output Amplifier

Convergence Output Amplifier Operation

The convergence output amplifiers convert the input correction voltage from the convergence adjustment circuit to a current to drive the convergence yoke. There are six convergence output amplifiers. All three of the vertical output amplifiers are the same, but the horizontal amplifiers differ slightly. All of the amplifiers use a push pull output stage with dual supplies to reduce power consumption. The vertical amplifiers use additional top and bottom output devices to provide a large output voltage swing for fast retrace. The red and blue horizontal output amplifiers only use a top boost device for retrace, and the green horizontal output amplifier does not require either a top or a bottom boost device. The blue vertical convergence output amplifier is covered since it is representative of all of the other five output amplifiers.

The input to the output amplifier is from the blue vertical convergence circuit. The signal is applied to an error amplifier in U7003. The output of the error amplifier is routed through Q7031. Q7031 is a common base amplifier. The signal at the collector has a constant DC level and variable current. The signal is then passed through another common base amplifier Q7032. The output at the collector of Q7032 is routed to the top and bottom output amplifiers. During scan, Q7034 and Q7035 provide the current through the convergence yoke. These transistors are supplied by the positive and negative 15 volt supplies. Diodes CR7046, CR7047, and CR7048 provide the bias for the output stages. The current sense output from the low side of the yoke provides negative feedback to the error amplifier.

During retrace, the additional output devices turn on to provide a large voltage swing for fast retrace. Zener diodes CR7051 and CR7054 provide a bias voltage which keeps the retrace output devices off during scan. At the beginning of retrace, the voltage at the top of the convergence yoke increases due to the collapsing field of the yoke. The additional voltage causes the retrace output devices to turn on, increasing the voltage across the yoke.

To troubleshoot malfunctions in the convergence output amplifiers, begin by grounding the input to the error amplifier. Ground the resistor at the end away form the error amplifier input. When the resistor is grounded, check for a 0 volt output at the top of the convergence yoke. Disconnect the yoke and check the 15 volt supplies. If the supplies are correct, substitute a 50 ohm 2 watt resistor for the yoke and check for 0 volts at the input to the yoke. If there is a DC offset suspect a malfunction in the biasing network, CR7046-7048, Q7032, or CR7069 and CR7070. Additionally, either the top or bottom scan output device could be shorted.

High Voltage Regulator Operation

The high voltage regulator develops a pulse which is applied to the low side of the high voltage winding. The amplitude of the pulse is varied by a control circuit. The control circuit compares the level of the high voltage to a fixed reference voltage. The regulator ensures that the level of the high voltage remains constant even if the beam current changes.

The high voltage supply decreases as the beam current increases. As the high voltage supply falls, the size of the raster increases. This occurs since the electron beam moves more slowly towards the face of the tube. The deflection yoke then has a greater effect on the beam. The beam is deflected more, and the picture appears to bend toward the edges of the tube. This effect is most apparent when viewing a scene with large changes in beam current as the beam moves down the face of the tube. The high voltage regulator circuit is needed in projection television since any error on the face of the CRT is magnified by the lens and mirror.

The circuit on the high voltage splitter SIP provides impedance matching and a voltage step down. The level of the high voltage is divided by a resistor divider network in the high voltage splitter. The sample voltage is routed through two buffer stages before it is sent to the high voltage regulator SIP. The voltage at the emitter of Q4702 is approximately 60 volts.

The sampled voltage is routed through another resistor divider network to provide the error signal input to a comparator in U4751. The other input to the comparator is a fixed reference voltage. The reference voltage is developed from t he 12-volt run supply by a 6.8-volt Zener diode CR4751. The output of the comparator is applied to the base of Q4753. Q4753 controls the turn on of Q4754 and Q4755. The Reg B+ supply is used to provide the power to both the buffer stage on the high voltage splitter SIP and the output stage on the high voltage regulator SIP. The Reg B+ is used to charge the capacitor connected at the emitters of Q4754 and Q4755. This capacitor provides the B+ for the MOSFET Q4752. When the high voltage needs to increase, Q4754 is turned on to charge the capacitor. When the high voltage needs to decrease, Q4755 is turned on to lower the charge on the capacitor.

The MOSFET is switched on and off at a horizontal rate by Q4751. Q4751 receives the horizontal drive pulses from U1001. Q4752 and the primary of T4751 form a resonant circuit similar to the horizontal deflection circuit. The circuit provides a pulse that occurs during horizontal retrace. The pulse is wider than the horizontal retrace pulse to ensure that the regulator pulses occur during horizontal retrace. The amplitude of the pulses is controlled by the charge on the capacitor. The pulses are coupled through T4751 to the bottom of the high voltage winding on the high voltage transformer.

The pulses are multiplied by the turns ratio of the high voltage transformer. The output of the high voltage regulator varies from 10 volts to 135 volts, and the change on the high voltage varies from 35 volts to 500 volts. At low beam current, the output of the regulator is minimum. As the beam current increases, the regulator causes the high voltage to increase.

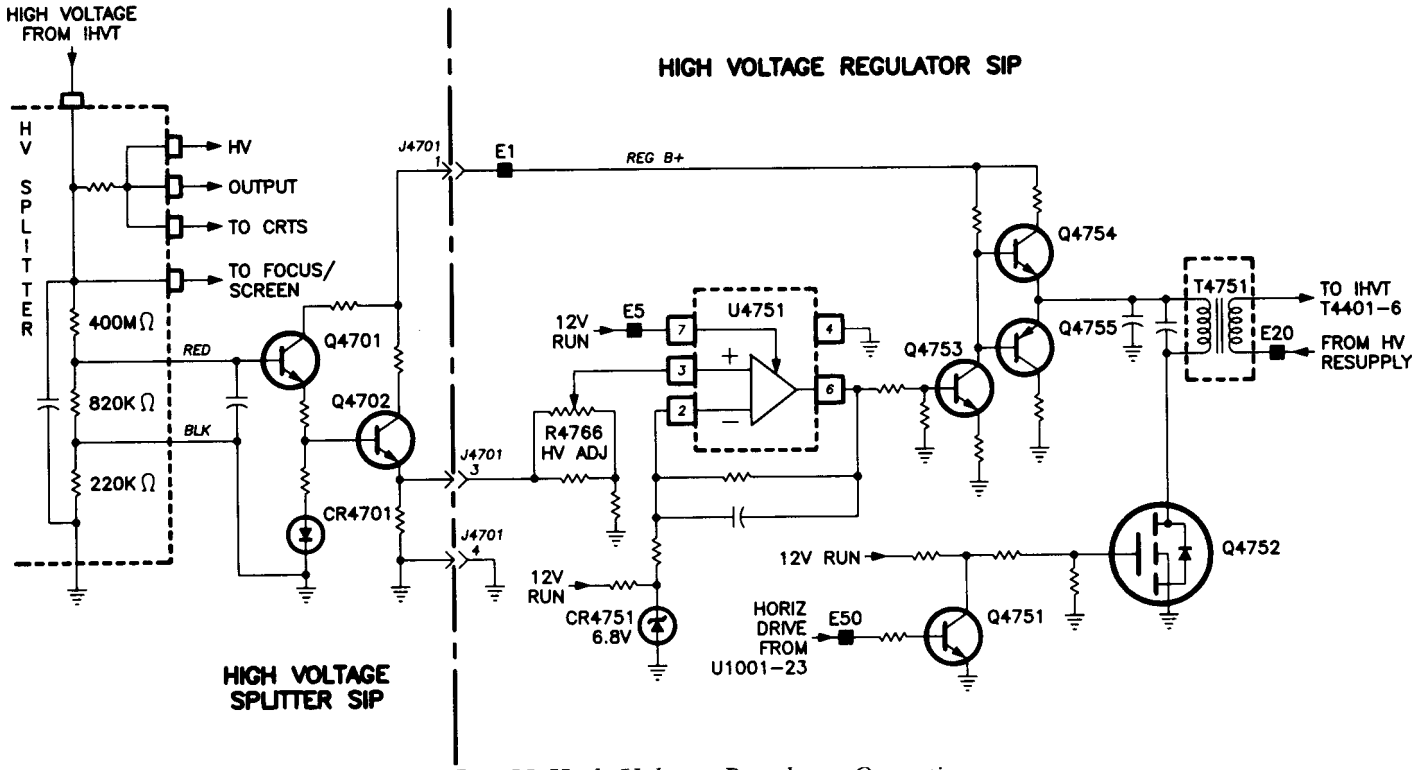


Fig. 55 High Voltage Regulator Operation

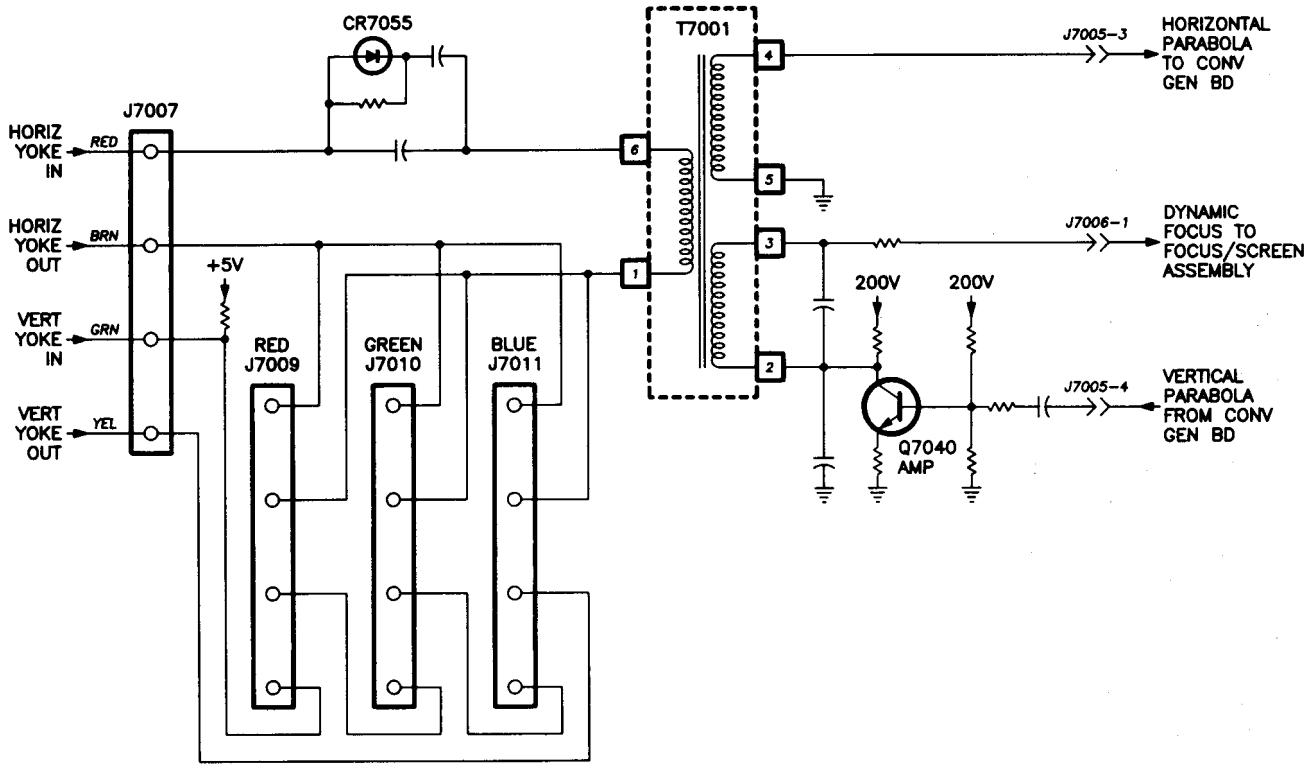


Fig. 56 Dynamic Focus Circuit

Dynamic Focus Operation

The dynamic focus circuit varies the focus voltage as the beam scans across the face of the CRT. The electron beam must be deflected more to strike the corner of the CRT than to strike the center. The focus tends to change slightly since the beam tends to spread in the corners due to the deflection angle. By varying the focus voltage at a horizontal and vertical rate, the focus can be kept constant as the beam crosses the face of the CRT.

The horizontal drive signal from the chassis is routed through the primary of T7001 before it is applied to the yoke connectors for the three CRTs. The horizontal deflection yokes are connected in parallel. T7001 has two secondary windings. One winding is used to couple the horizontal dive signal to the convergence generator board. This output is a horizontal parabola without the "S" correction, and is used for vertical bow and linearity correction.

The second winding of T7001 combines the horizontal parabola with a vertical rate parabola. The resulting signal is applied to the focus/screen assembly. The vertical parabola from the convergence generator is amplified by Q7040. The output of the amplifier is added to the horizontal parabola and routed to the focus assembly.

Scan Loss Detection Circuit Operation

The scan loss detection circuit provides protection for the CRTs. In projection television receivers, the CRTs are driven harder than direct view CRTs. If the deflection circuit stops operating, the video drive to the CRT does not stop instantly. The phosphor coating on the CRT can be burned if the electron beam is not moved across the face of the CRT. The scan loss detection circuit operates if either the horizontal or vertical scan stops operating. The circuit removes the drive from the CRT to prevent burning the face of the CRT.

The inputs to the scan loss detector are the vertical parabola from the yoke windings and the heater pulses from the high voltage transformer. The heater pulses are a horizontal rate signal and the high voltage transformer is driven by the horizontal output transistor. If there is a problem with the horizontal scan, the heater pulses will either be missing or too small to keep the scan on. The output of the detector circuit is connected to all three of the CRT driver boards. The output is low during normal operation and is pulled high by the circuit on the CRT socket board whenever the loss of scan is detected.

The heater pulses from the high voltage transformer are rectified by CR7078 and applied to the emitter of Q7043. The base of Q7043 is biased by the reference voltage provided by CR7080. When the heater pulses are present, Q7043 is on, and the voltage at the non inverting input of the comparator is higher than the reference voltage. The output of the comparator at pin 1 is high when the heater pulses are present.

The vertical scan input is the vertical drive voltage from the yoke. The vertical signal is coupled through a capacitor to the junction of two Shotkey diodes. These diodes were chosen for the lower forward voltage drop. When the vertical scan is present, the voltage at the non inverting input of the comparator is higher than the voltage at the inverting input. The voltage at the inverting input is provided by CR7080. When the vertical scan is present, a high is present at the output of the comparator.

When both the horizontal and vertical scans are present, the output of both comparators is high. Q7044 is biased on by the high on the base. When Q7044 is on, the voltage at the base of Q7042 is pulled to approximately 10 volts. The output of the comparator is approximately 15 volts. The voltage at the emitter of Q7042 is approximately 15 volts, and so Q7042 is biased on. When Q7042 is on, the voltage at the base of Q7048 is high, causing it to turn on. When Q7048 is on, the voltage at the collector is approximately zero. This allows the CRT drivers to operate normally.

If either of the comparator outputs change to a low, Q7048 is turned off. When Q7048 is off, the scan loss circuits on the kine socket boards are activated. The CRT drive voltage is removed from the tubes.

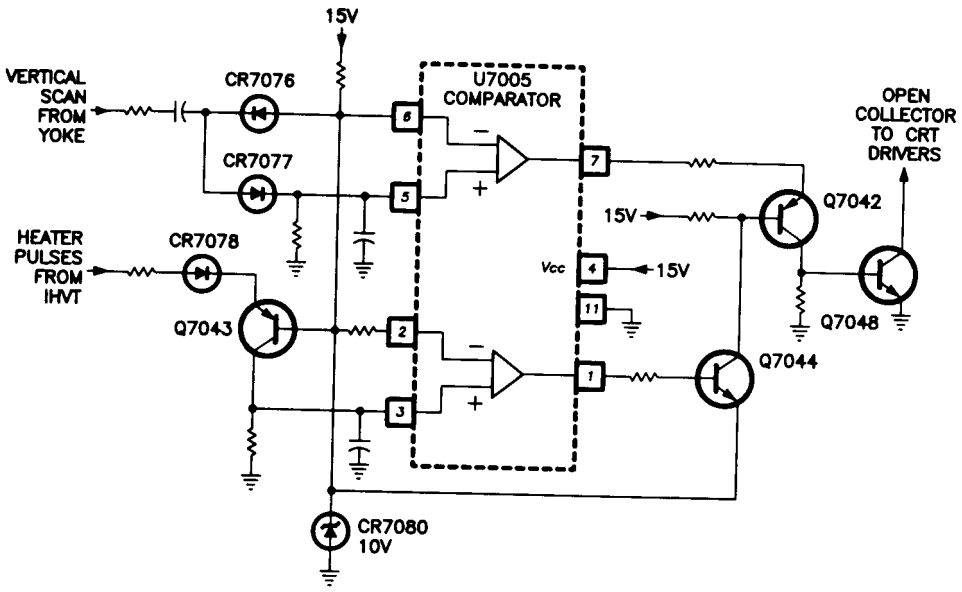


Fig. 57 Scan Loss Detection Circuit

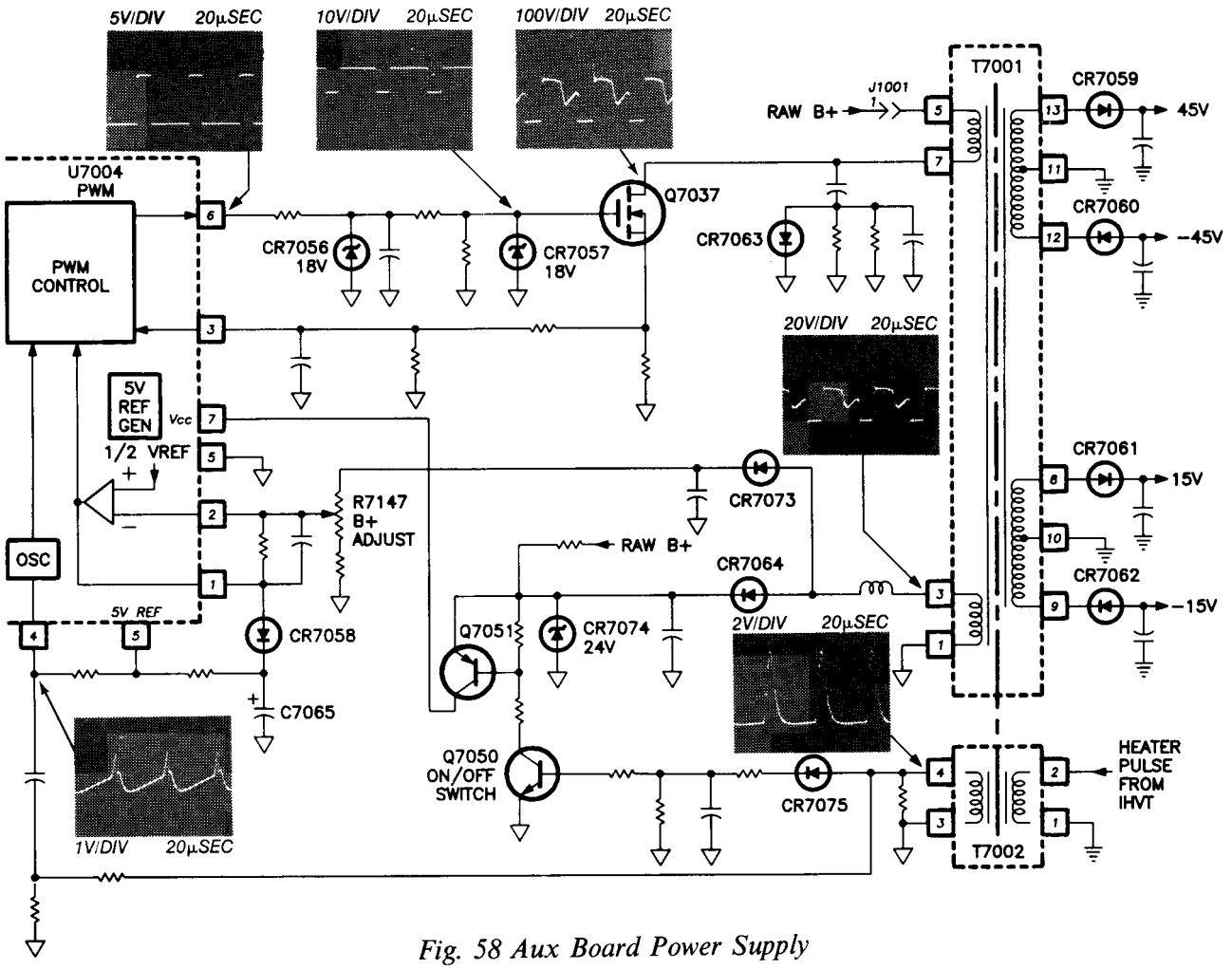


Fig. 58 Aux Board Power Supply

Aux Board Power Supply Operation

A separate switched mode power supply is used to provide power for the circuits contained on the PTV Aux board. These circuits include the convergence generator and convergence output amplifiers. The switching regulator is very similar to the supply used in the CTC149 chassis for the 5-watt-per channel stereo audio amplifier. The regulator in the projection receivers is a 50-watt supply and provides both positive and negative 45V and 15V outputs.

Power Supply Startup

The raw B+ is routed from the chassis to the aux board. The raw B+ is applied to the drain of Q7037 through the primary of T7001. In addition, the raw B+ is applied through a dropping resistor to the emitter of Q7051. The on/off operation of the power supply is controlled by the horizontal circuit on the chassis. Heater pulses from the high voltage transformer are coupled through T7002. The pulses are rectified and the DC voltage is used to turn on Q7050. When Q7050 is on, the voltage at the base of Q7051 is lower than the voltage at the emitter, allowing Q7051 to conduct. The voltage is applied to the Vcc input of U7004 at pin 7. The IC contains an under voltage lock out circuit which prevents the IC from operating until the voltage at pin 7 rises above the trigger level (14.5V to 17.5V).

The soft start circuit (CR7058 and C7065) prevents the power supply from starting at its maximum duty cycle. The output of the error amplifier is shunted from pin 1 through CR7058 to C7065. C7065 charges from the 5V reference output at pin 8, and CR7058 becomes reverse biased. The output of the error amplifier ramps up slowly and the power supply starts gently.

When the power supply begins operation, the oscillator circuit begins to operate. The heater pulses from the high voltage transformer are coupled to pin 4 of the IC to lock the oscillator to the horizontal frequency. When the oscillator begins to operate, the PWM controller produces a square wave output. The output pulses from pin 6 drive the gate of Q7057 on and off. Since raw B+ is applied to the drain of Q7057, output pulses are produced and coupled across T7001 to the output windings and the feedback/run winding.

The output of the feedback/run winding is rectified by CR7073 to provide feedback voltage to the IC. The output of the winding is also rectified by CR7064 to provide the run Vcc to pin 7 of the IC. The run Vcc is between

12.5 and 15 volts. The run voltage is below the under voltage lock out turn on voltage but above the turn off voltage of 8.5 to 11.5 volts. The current from the raw B+ supply is limited by the dropping resistor, but the capacitor at the emitter of Q7051 supplies the current to the IC until the run supply is up.

Power Supply Regulation

The power supply is a current-mode pulse width modulator. The regulator compares a voltage that represents the output current with the voltage output of the error amplifier. The resistor at the source of Q7037 develops a voltage that is proportional to the current through Q7037. The current sense voltage is filtered and passed to the current sense input at U7004-3. A triangle wave voltage appears at pin 3. The PWM controller begins each output pulse as timed by the oscillator circuit. The pulse ends when the current sense input equals the output of the error amplifier.

When the load on the secondaries of T7001 increases, the output voltage drops. The supply draws more current from the transformer. This reduces the energy available for the feedback winding and so the feedback voltage decreases. The error amplifier detects the decrease in feedback voltage and the error voltage output is increased. The turn on time of Q7037 is fixed by the oscillator and is tied to the horizontal. The turn off time occurs when the current sense input equals the error voltage. Since the error voltage has increased, Q7037 must remain on longer for the current sense voltage to reach the error voltage. Q7037 stays on longer, transferring more energy to the secondary.

Overcurrent Protection

The current sense input at U7004-3 is also used to detect overcurrent conditions in the power supply. If the current sense voltage rises excessively (indicating an overcurrent condition), the PWM controller stops the output of the gate drive pulse from pin 6. The power supply will then pulse on and off at 1/2-second intervals until the overcurrent condition is eliminated.

Troubleshooting Strategies

Problems in the aux board power supply are sometimes difficult to diagnose since the switching regulator on the chassis and the aux board power supply can cause the same symptom. There is only one fuse on the main chassis, and a short on the chopper output device or a shorted output FET in the aux board power supply causes the line fuse to open. The surge resistor on the chassis is also likely to open. In the event of an open fuse or surge resistor, disconnect the raw B+ input to the aux board and measure the resistance from the raw B+ to hot ground. If the resistance is less than one megohm, suspect a short or leakage in Q7037, T7001, or the snubber network. If the resistance is greater than one megohm, suspect a malfunction in the chopper supply on the main chassis. The set can be turned on with the raw B+ to the aux board disconnected. The screen will be blanked since the scan loss detect circuit is turned on. The audio operates normally. If the audio operates normally and the chopper supply produces the correct reg B+, the malfunction must be in the aux board power supply. If the audio is not correct, the problem is on the chassis and the aux board power supply is probably operating normally.

If the raw B+ and the heater pulses are present and the power supply is pulsing on and off, suspect loss of feedback/run Vcc or overcurrent shutdown.

- If the feedback/run Vcc is missing, the voltage at pin 7 of U7004 will cycle above the under voltage lock out point (greater than 14.5 volts) to below the turn off voltage (less than 11.5 volts). Suspect an open CR7073 or a leaky capacitor.
- If an overcurrent shutdown is suspected, suspect a short or leakage in CR7059, CR7060, CR7061, or CR7062, a filter capacitor, or a shorted convergence output amplifier.

A short circuit or severe leakage in T7001 can also cause an overcurrent shutdown. This condition is difficult to detect because all windings have very low resistance. The process of elimination must be used to determine if T7001 is at fault. All other components in the power supply must be checked before T7001 is replaced. If any measurable resistance occurs between any of the windings of T7001 when T7001 is measured out of the circuit, T7001 should be replaced.

APPENDIX A

U3101 SYSTEM CONTROL/OSD MICRO

PIN NO.	I/O	SIGNAL NAME	IN CKT RES.	DESCRIPTION
1	I	$\overline{\text{PWR-ON RESET}}$	10K	Micro reset - Active Low.
2	I	$\overline{\text{FAULT DET}}$	15K	When a low is sensed at this input, system control turns the set off for two seconds and turns it back on. If pin 2 goes low three times in one minute, system control keeps the set off.
3	I	IR	38K	Receives 5 Vp-p IR signal from remote receiver.
4	O	VERT KILL/ DEGAUSS	>20M	Goes high to kill vertical deflection during degaussing and the service line in direct view sets.
5	I	$\overline{\text{KS3}}$	900K	Keyboard scan input.
6	I	$\overline{\text{KS2}}$	900K	Keyboard scan input.
7	I	$\overline{\text{KS1}}$	900K	Keyboard scan input.
8	I	$\overline{\text{KS0}}$	900K	Keyboard scan input.
9	O	AUX 2	>20M	Video select control line.
10	O	AUX 1	>20M	Video select control line.
11	O	$\overline{\text{KD1}}$	10K	Keyboard scan output.
12	I/O	$\overline{\text{KD3}}$/ TUNING SYNC	9K	Keyboard scan output/tuning sync input.
13	O	ENABLE	>20M	Serial communications control line which goes high during data transmission and low during address transmission.
14	I/O	DATA	111K	Serial communications data line.
15	O	CLOCK	>20M	Serial communications clock line.
16	I	BLUE	16M	Blue OSD output. Active high.
17	I	GREEN	14M	Green OSD output. Active high.
18	I	RED	11M	Red OSD output. Active high.
19	-	VDD	1.4M	+5 VDC.
20	-	VSS	0	GND.
21	O	$\overline{\text{BLNK}}$	>20M	OSD black surround out. Low = Black.
22	O	$\overline{\text{SYS RST}}$	>20M	System reset line connected to bus devices. Goes low when set is off and high when set is on.
23	I	H-SYNC	16K	Horizontal timing input for OSD.
24	I	V-SYNC	11K	Vertical timing input for OSD.
25	-	R1	10K	OSD PLL external control pin.
26	-	VCO	>20M	OSD VCO external control pin.
27	O	SPKRS OFF	110K	Goes high to turn speakers off and low to turn them on.
28	O	$\overline{\text{RFSW/MONO}}$	>20M	RF switch control line. Low selects Ant. A. Mono function currently not used.
29	O	TV PIX	>20M	Goes high when TV tuner is selected and low when external video is selected.
30	O	VOLUME	>20M	PWM for Volume control (currently not used).
31	O	TINT	11K	PWM for Tint control.
32	O	COLOR	19K	PWM for Color control.
33	O	CONTRAST	33K	PWM for Contrast control.
34	O	BRIGHTNESS	97K	PWM for Brightness control.
35	O	SHARPNESS	12K	PWM for Sharpness control.
36	I/0	CH CHG/AFT REF	105K	At start of channel change, voltage at pin 36 is read by micro for use in AFT A/D converter. During channel change, line goes high until channel change is executed.
37	I	AFT	73K	Automatic fine tuning input. Crossover point detected at 2.5 VDC.
38	O	TV ON	>20M	Power ON/OFF control. High = ON, Low = OFF.
39	O	OSC OUT	5M	4 MHz oscillator output.
40	I	OSC IN	4M	4 MHz oscillator input.

APPENDIX B

U1001 CTV PROCESSOR (ONE-CHIP)

PIN NO.	I/O	SIGNAL NAME	IN CKT RES.	DESCRIPTION
1	O	AUDIO OUT	>20M	Not used.
2	O	RF AGC OUT	69K	RF gain control voltage for tuner.
3	I	RF AGC IN	2.3K	Adjusts the operation point of the RF AGC circuit.
4	-	SIF DET	>20M	Connection for audio detection tank.
5	-	PIF AGC1	>20M	High frequency IF AGC filter.
6	I	EXT AUDIO IN	37K	Not used.
7	-	PIF AGC2	>20M	Low frequency IF AGC filter and IF defeat connection point.
8	-	P/S GND	0	PIF/SIF ground.
9	I	IF IN	20K	IF input from SAW filter.
10	I	IF IN	20K	IF input from SAW filter.
11	I	FC ADJUSTMENT	41K	Chroma oscillator and filter adjustment.
12	-	APC FILTER	>20M	Controls phase (tint) of chroma signal.
13	-	X'TAL 3.58	>20M	3.58 MHz chroma oscillator.
14	I	V/C/D VCC	1.8K	9 VDC VCC for video, chroma, and deflection circuits within U1001.
15	O	R-Y	4.3K	R-Y color difference signal output.
16	O	-Y	1.5M	Luminance output.
17	O	G-Y	4.2K	G-Y color difference signal output.
18	O	B-Y	4.2K	B-Y color difference signal output.
19	I	RED OSD	>20M	Red OSD input which is connected to the Blank (bar) line from system control to produce the black border around OSD characters.
20	I	GREEN OSD	>20M	Not used.
21	I	F B PULSE	>20M	Input for chroma burst amp and horizontal centering control.
22	I	X-RAY PROTECT	32K	When voltage at this pin reaches approximately 1.5 VDC, X-Ray protect activates and stops horizontal drive pulses from pin 23 of U1001.
23	O	H OUT	440ohm	Horizontal output pulses which are applied to the horizontal deflection stage.
24	I	H AFC	>20M	Horizontal AFC input.
25	-	32H OSC	>20M	503 kHz oscillator for horizontal countdown stage.
26	I	H VCC	81K	VCC for sync stages.
27	O	V OUT	1K	Not used.
28	-	V NFB	49K	Negative feedback for vertical ramp stage.
29	0	V RAMP	3.2K	Vertical reset output applied to vertical deflection stage.
30	-	COLOR KILLER	2.7M	Disables chroma circuits when chroma burst is not received. Color killer activates at about 6.5 VDC at pin 30.
31	I	TV/EXT SW CHROMA IN	40K	Chroma input in addition to control line for TV/EXT video switching at pins 40 and 43. DC level of chroma signal is used to perform the switching. With TV video selected, DC offset is about 4.5 VDC and 1.2 VDC with external video selected.
32	I	S-VHS SW	0	Not used.
33	-	OSD BRIGHT	1.8K	Voltage at this pin is transferred to the -Y output of U1001 whenever the Red OSD pin 19 is pulled low. This technique is used to produce the black border around the OSD characters.
34	I	SHARP	17K	DC control and high frequency luma input for sharpness control. 5.8 VDC to 7.9 VDC min to max (approx).
35	I	DELAYED VIDEO	210K	Delayed low frequency luma input for sharpness control circuit.

U1001 CTV PROCESSOR (ONE-CHIP) Continued

PIN NO.	I/O	SIGNAL NAME	IN CKT RES.	DESCRIPTION
36	I	BRIGHT CTRL	16K	DC control input for brightness. 5.2 VDC - 5.6 VDC min to max (approx).
37	O	V SEP FILTER	>20M	In this application, this luma output is used to provide signal to the scan velocity modulation circuit (SVM).
38	O	VIDEO OUT	3.3K	Luma output of contrast control amp.
39	-	V/C/D GND	0	Ground for video, chroma, and deflection circuits within U1001.
40	I	EXT VIDEO	>20M	Luma input for video source other than TV tuner.
41	I	CONT CTRL	15K	DC control input for contrast. 4.4 VDC - 6.5 VDC min to max (approx).
42	I	COLOR	>20M	DC control input for color level. 3.0 VDC - 5.0 VDC min to max (approx).
43	I	VIDEO IN	>20M	Luma input used for TV tuner source only.
44	I	TINT CTRL	33K	DC control input for tint. 3.2 VDC -5.9 VDC red to green (approx).
45	O	VIDEO DET OUT	>20M	Composite video output of IF video detector.
46	I	P/C VCC	1.8K	VCC for Pix IF and Sound IF circuits.
47	-	PIF	3.6K	Connection for video detector tank.
48	-	PIF	3.6K	Connection for video detector tank.
49	-	AFT TANK	>20M	Connection for AFT tank.
50	O	AFT OUT	91K	AFT output to system control micro which swings from 0 to 9 VDC. Divided down to 0 to 5 VDC swing for system control micro AFT input. Nominal tuning represented by 2.5 VDC at AFT input of system control micro U3101.
51	I	SIF INPUT	2.9K	4.5 MHz input for sound IF circuit.
52	O	WIDE BAND AUDIO OUTPUT	35K	Wide band audio output of FM sound detector.The audio at this output is not volume controlled.
53	I	EXT AUDIO IN	39K	Not used.
54	I	EXT AUDIO ATTEN CONTROL	>20M	Not used.

APPENDIX C
CTC168/169 TUNING TABLE (CATV)

RCA NO.	CH NO.	BAND	PIX FREQ. MHZ	LOCL OSC MHZ
2	2	0	55.25	101
3	3	0	61.25	107
4	4	0	67.25	113
1	4A	0	73.25	119
5	5	0	77.25	123
6	6	0	83.25	129
6 IRC	A-6	0	85.25	131
95	A-5	0	91.25	137
96	A-6	0	97.25	143
97	A-3	0	103.25	149
98	A-2	0	109.25	155
99	A-1	0	115.25	161
14	A	0	121.25	167
15	B	0	127.25	173
16	C	0	133.25	179
17	D	0	139.25	185
18	E	1	145.25	191
19	F	1	151.25	197
20	G	1	157.25	203
21	H	1	163.25	209
22	I	1	169.25	215
7	7	1	175.25	221
8	8	1	181.25	227
9	9	1	187.25	233
10	10	1	193.25	239
11	11	1	199.25	245
12	12	1	205.25	251
13	13	1	211.25	257
23	J	1	217.25	263
24	K	1	223.25	269
25	L	1	229.25	275
26	M	1	235.25	281
27	N	1	241.25	287
28	O	1	247.25	293
29	P	1	253.25	299
30	Q	1	259.25	305
31	R	1	265.25	311
32	S	1	271.25	317
33	T	1	277.25	323
34	U	1	283.25	329
35	V	1	289.25	335
36	W	1	295.25	341
37	W+1	1	301.25	347

RCA NO.	CH NO.	BAND	PIX FREQ. MHZ	LOCL OSC MHZ
38	W+2	1	307.25	353
39	W+3	1	313.25	359
40	W+4	1	319.25	365
41	W+5	1	325.25	371
42	W+6	1	331.25	377
43	W+7	1	337.25	383
44	W+8	1	343.25	389
45	W+9	1	349.25	395
46	W+10	1	355.25	401
47	W+11	1	361.25	407
48	W+12	1	367.25	413
49	W+13	1	373.25	419
50	W+14	1	379.25	425
51	W+15	1	385.25	431
52	W+16	1	391.25	437
53	W+17	1	397.25	443
54	W+18	1	403.25	449
55	W+19	1	409.25	455
56	W+20	1	415.25	461
57	W+21	2	421.25	467
58	W+22	2	427.25	473
59	W+23	2	433.25	479
60	W+24	2	439.25	485
61	W+25	2	445.25	491
62	W+26	2	451.25	497
63	W+27	2	457.25	503
64	W+28	2	463.25	509
65	W+29	2	469.25	515
66	W+30	2	475.25	521
67	W+31	2	481.25	527
68	W+32	2	487.25	533
69	W+33	2	493.25	539
70	W+34	2	499.25	545
71	W+35	2	505.25	551
72	W+36	2	511.25	557
73	W+37	2	517.25	563
74	W+38	2	523.25	569
75	W+39	2	529.25	575
76	W+40	2	535.25	581
77	W+41	2	541.25	587
78	W+42	2	547.25	593
79	W+43	2	533.25	599
80	W+44	2	559.25	605

RCA NO.	CH NO.	BAND	PIX FREQ. MHZ	LOCL OSC MHZ
81	W+45	2	565.25	611
82	W+46	2	571.25	617
83	W+47	2	577.25	623
84	W+48	2	583.25	629
85	W+49	2	589.25	635
86	W+50	2	595.25	641
87	W+51	2	601.25	647
88	W+52	2	607.25	653
89	W+53	2	613.25	659
90				
91				
92				
93	W+57	2	637.25	683
94	W+58	2	643.25	689
100	W+59	121	649.25	695
101	W+60	2	655.25	701
102	W+61	2	661.25	707
103	W+62	2	667.25	713
104	W+63	2	673.25	719
105	W+64	2	679.25	725
106	W+65	2	685.25	731
107	W+66	2	691.25	737
108	W+67	2	697.25	743
109	W+68	2	703.25	749
110	W+69	2	709.25	755
111	W+70	2	715.25	761
112	W+71	2	721.25	767
113	W+72	2	727.25	773
114	W+73	2	733.25	779
115	W+74	2	739.25	785
116	W+75	2	745.25	791
117	W+76	2	751.25	797
118	W+77	2	757.25	803
119	W+78	2	763.25	809
120	W+79	2	769.25	815
121	W+80	2	775.25	821
122	W+81	2	781.25	827
123	W+82	2	787.25	833
124	W+83	2	793.25	839
125	W+84	2	799.25	845
126	W+54	2	619.25	665
127	W+55	2	625.25	671
128	W+56	2	631.25	677

APPENDIX C (cont.)
CTC168/169 TUNING TABLE (AIR)

CH NO.	BAND	PIX FREQ. MHZ	LOCL OSC MHZ
2	0	55.25	101
3	0	61.25	107
4	0	67.25	113
5	0	77.25	123
6	0	83.25	129
7	1	175.25	221
8	1	181.25	227
9	1	187.25	233
10	1	193.25	239
11	1	199.25	245
12	1	205.25	251
13	1	211.25	257
14	2	471.25	517
15	2	477.25	523
16	2	483.25	529
17	2	489.25	535
18	2	495.25	541
19	2	501.25	547
20	2	507.25	553
21	2	513.25	559
22	2	519.25	565
23	2	525.25	571

CH NO.	BAND	PIX FREQ. MHZ	LOCL OSC MHZ
24	2	531.25	577
25	2	537.25	583
26	2	543.25	589
27	2	549.25	595
28	2	555.25	601
29	2	561.25	607
30	2	567.25	613
31	2	573.25	619
32	2	579.25	625
33	2	585.25	631
34	2	591.25	637
35	2	597.25	643
36	2	603.25	649
37	2	609.25	655
38	2	615.25	661
39	2	621.25	667
40	2	627.25	673
41	2	633.25	679
42	2	639.25	685
43	2	645.25	691
44	2	651.25	697
45	2	657.25	703
46	2	663.25	709

CH NO.	BAND	PIX FREQ. MHZ	LOCL OSC MHZ
47	2	669.25	715
48	2	675.25	721
49	2	681.25	727
50	2	687.25	733
51	2	693.25	739
52	2	699.25	745
53	2	705.25	751
54	2	711.25	757
55	2	717.25	763
56	2	723.25	769
57	2	729.25	775
58	2	735.25	781
59	2	741.25	787
60	2	747.25	793
61	2	753.25	799
62	2	759.25	805
63	2	765.25	811
64	2	771.25	817
65	2	777.25	823
66	2	783.25	829
67	2	789.25	835
68	2	795.25	841
69	2	801.25	847

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The CTC 168/169

Technical Training Workbook

RCA

Color Television Receivers

EXERCISE ONE

Purpose: the purpose of this exercise is to provide the technician with a review of basic troubleshooting concepts and the application of these concepts to malfunctions in the startup and B+ regulator circuits.

The basic concepts of troubleshooting require that some steps be taken before components are replaced. Begin by confirming that the set is properly connected and adjusted for normal operation. Perform a complete operational check. Verify the reported symptom and record any other symptoms that appear. It is important to classify the symptom. The chassis can be divided into five major circuit areas. Try to sectionalize the symptom into one of the five areas. These areas are:

- Power Supply
- System Control/Tuning
- Signal Processing
- Deflection
- Audio

Normally, verifying the reported symptom enables the technician to sectionalize the malfunction to one of these circuit areas before removing the back cover. For example, if the audio is normal but the screen is blank, the problem is most likely to be in the signal processing section.

1. Which of the five major circuit areas could cause a dead set symptom? Check all that apply.

   _____ Power Supply

   _____ System Control/Tuning

   _____ Signal Processing

   _____ Deflection

   _____ Audio

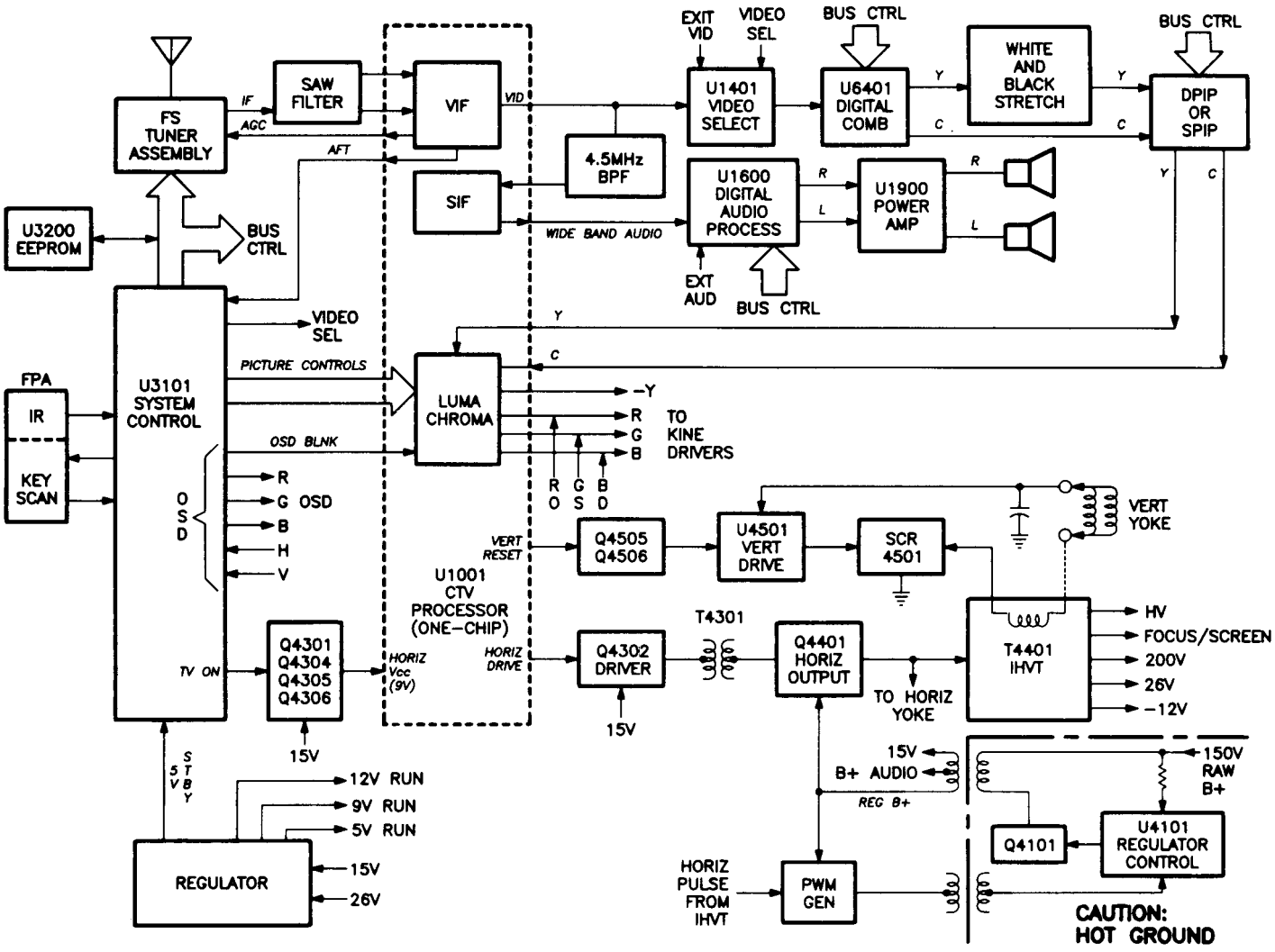

Fig. 1 Simplified Block Diagram

2. The switching regulator is used to provide both the standby and run B+ supplies. When troubleshooting a dead set symptom, the TV ON output from the system control microcomputer was found to be normal. Which of the following major circuit areas could now be eliminated as the probable cause of the malfunction? Check all that apply.

_____ Standby Power Supply

_____ System Control/Tuning

_____ Signal Processing

_____ Deflection

_____ Audio

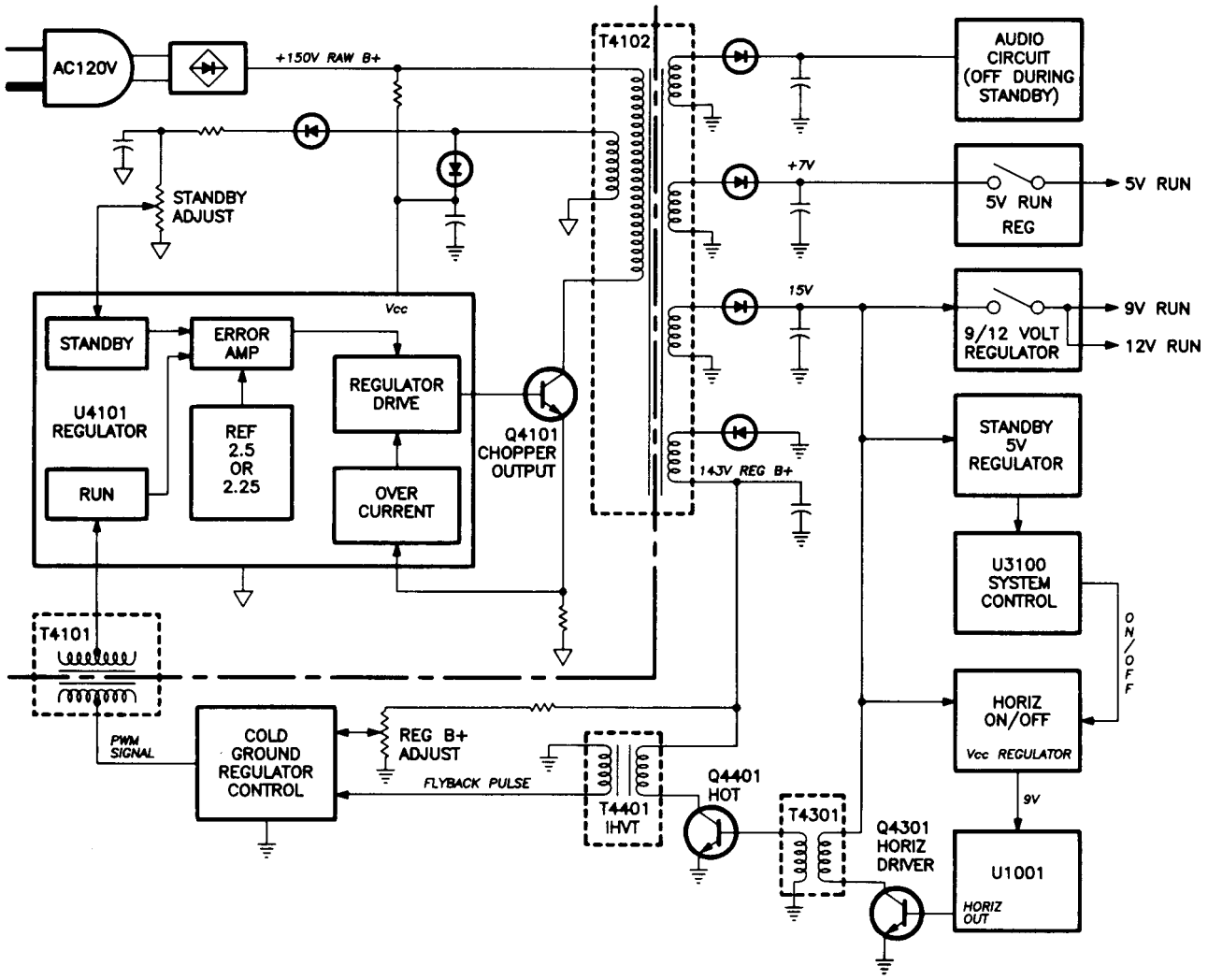

Fig. 2 B+ Regulator Block Diagram

3. The B+ regulator has two modes of operation, standby and run. In the standby mode, what input is monitored to regulate the Reg B+ supply?

   _____ PWM signal from the cold ground regulator control

   _____ Overcurrent sense input from Q4101E

   _____ Vcc input to U4101

   _____ DC input from the wiper of the standby adjust pot

4. What input is monitored to regulate the 143V reg B+ supply in the run mode?

   _____ PWM signal from the cold ground regulator control

   _____ Overcurrent sense input from Q4101E

   _____ Vcc input to U4101

   _____ DC input from the wiper of the standby adjust pot

5. What symptom would you expect if the PWM input was missing?

_____ Dead Set

_____ XRP shutdown

_____ Set operates but raster size changes with changes in scene content

_____ Set operates normally

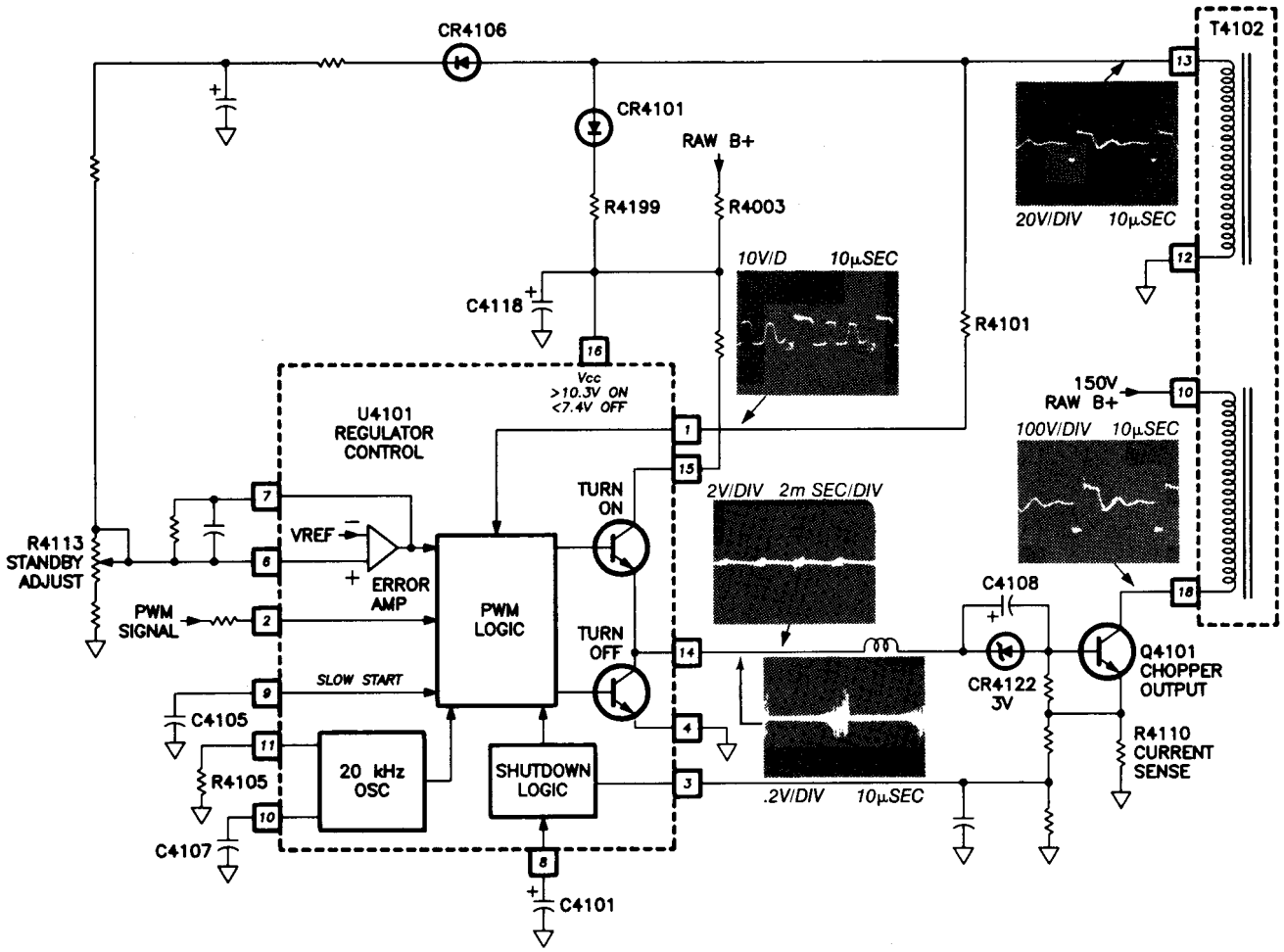

Fig. 3 B+ Regulator Standby Circuit

6. There are three different shutdown modes which can cause a shutdown symptom. These are overcurrent, X-ray, and overvoltage. Which of the shutdown modes would you suspect if the standby supplies were present but the set exhibited a shutdown symptom?

_____ Overcurrent

_____ X-ray protection

_____ Overvoltage

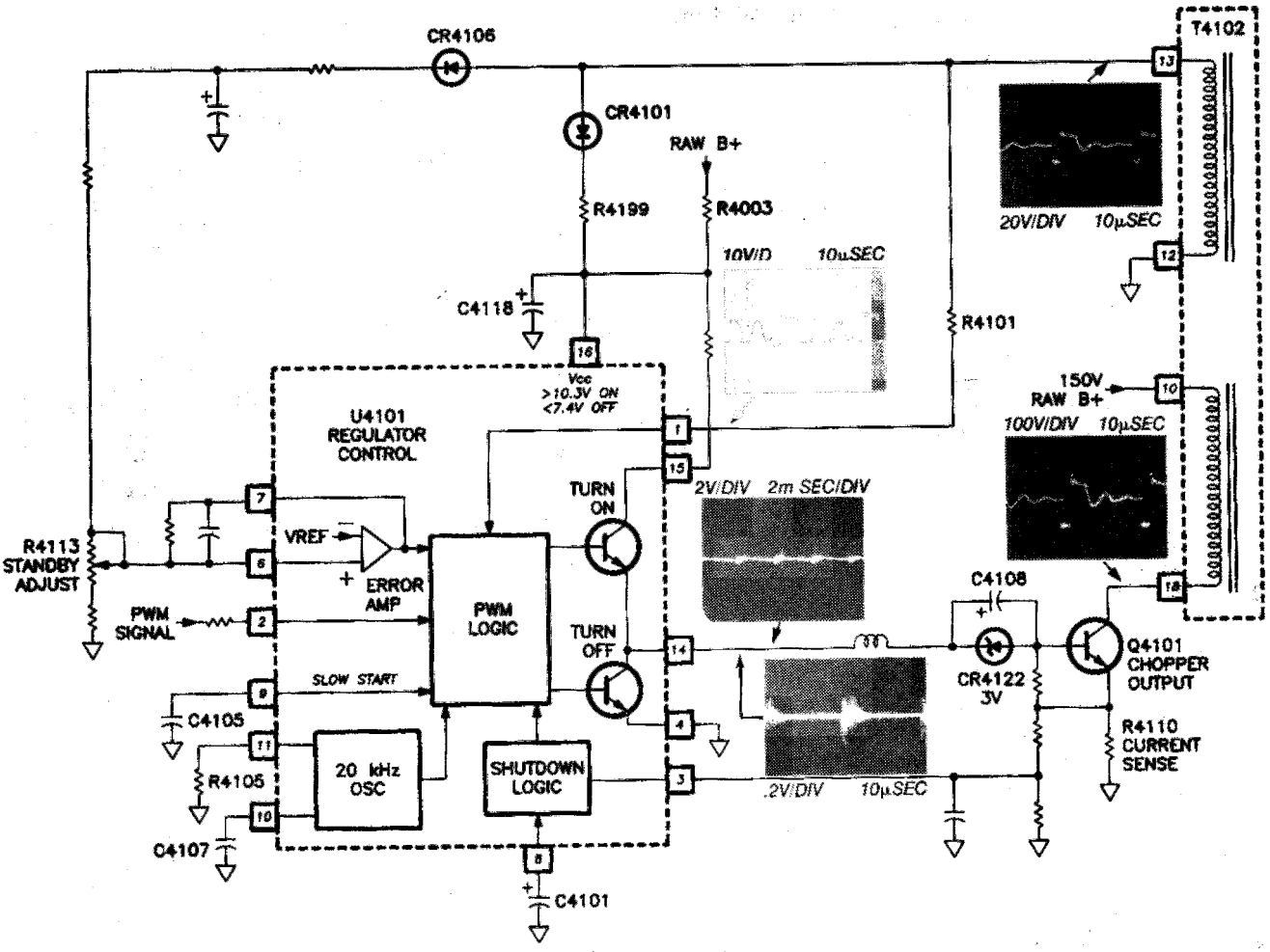

Fig. 3 B+ Regulator Standby Circuit

7. The run B+ supply for the regulator control IC is provided from pin 13 of T4102 through CR4101 to pin 16 of U4101. U4101 enters the overvoltage shutdown mode if the input voltage at pin 16 rises above approximately 15 volts. What symptom would you expect if CR4106 opened?

_____ Reg B+ would be too low

_____ Overvoltage shutdown

_____ Overcurrent shutdown

_____ X-ray shutdown

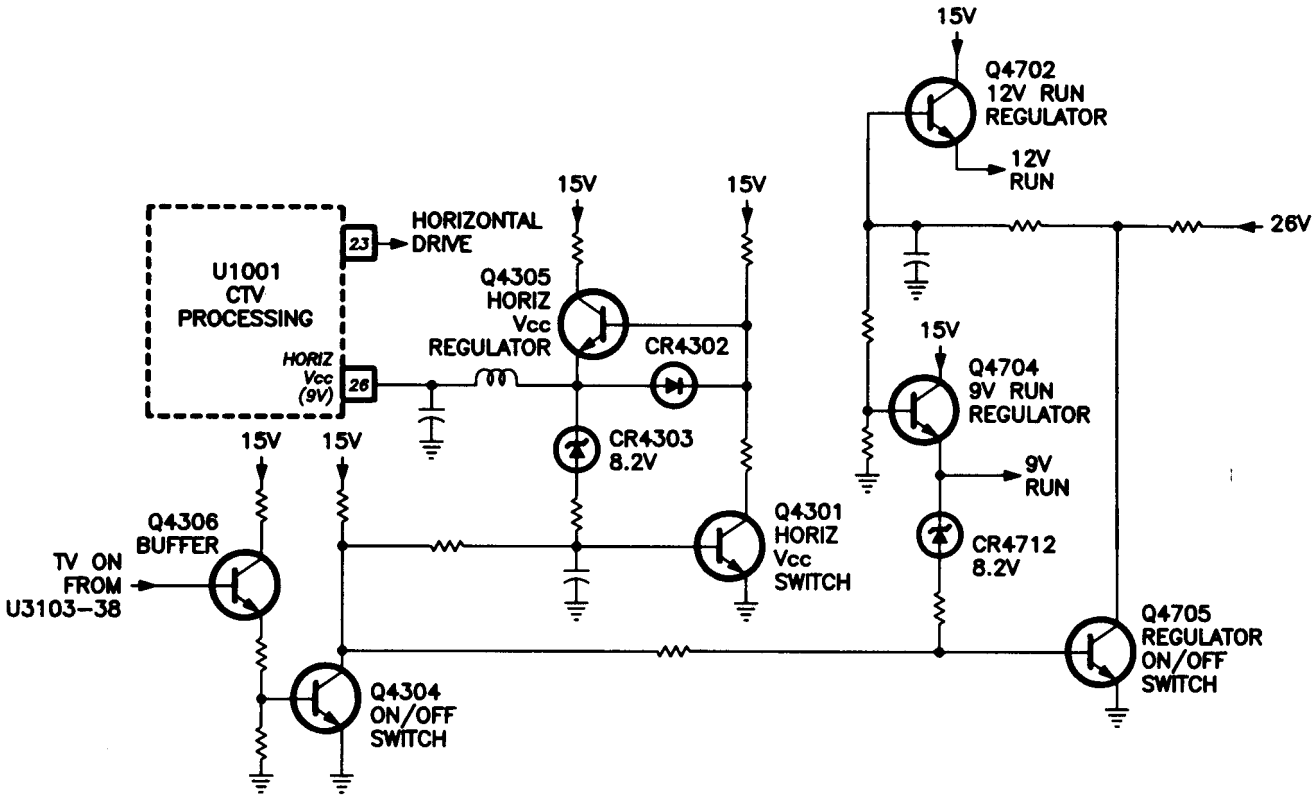

Fig. 4 On/Off Circuit

8. The on/off operation of the chassis is controlled by the system control microcomputer. If the microcomputer was suspected as the cause of a dead set symptom, how could you substitute for the system control circuit and force the chassis to turn on?

   _____ Ground the base of Q4306

   _____ Ground the base of Q4304

   _____ Ground the collector of Q4304

   _____ Apply an external 26 volt supply

9. If the horizontal deflection circuit fails to operate, will the 9-volt and 12-volt run supplies be present? Why or why not?

   _____

   _____

   _____

EXERCISE TWO

Purpose: The purpose of this exercise is to provide the technician with troubleshooting hints for the vertical deflection circuit of the CTC168/169 color television chassis.

1. The operation of the vertical deflection circuit is in many ways similar to the operation of a switching power supply. The horizontal rate pulses from T4401 are rectified by CR4504. The DC voltage is used to charge C4511. What is the purpose of SCR501?

   _____

   _____

   _____

2. The horizontal rate pulses from T4401-7 are rectified by CR4502 to provide the charge current for ramp capacitor C4519. What is the purpose of ramp reset switch Q4505?

   _____ Change the picture height

   _____ Discharge the ramp capacitor during retrace

   _____ Provide correction for pincushion distortion

   _____ Raise the cost of the chassis

3. What symptom would you expect if the vertical reset pulse was missing?

   _____

4. What symptom would you expect if zener diode CR4512 was leaky?

   _____

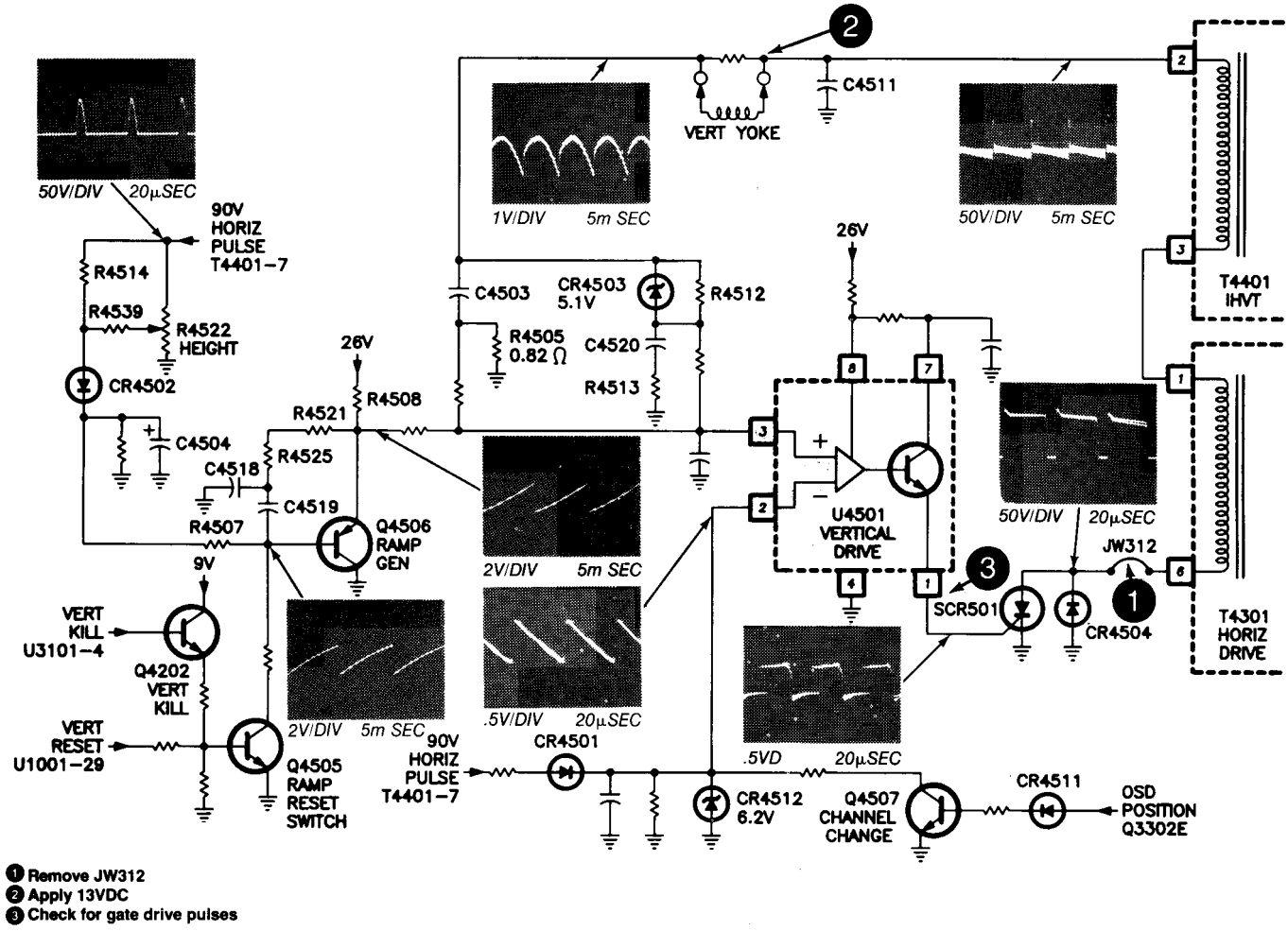

Fig. 5 Vertical Deflection Circuit

5. What symptom would you expect if SCR501 never received a gating pulse to cause it to turn on?

_____ No vertical scan

_____ Dead Set

_____ Increased vertical scan

_____ X-ray shutdown

6. What symptom would you expect if CR4504 was shorted?

_____ No vertical scan

_____ Dead Set

_____ Increased vertical scan

_____ X-ray shutdown

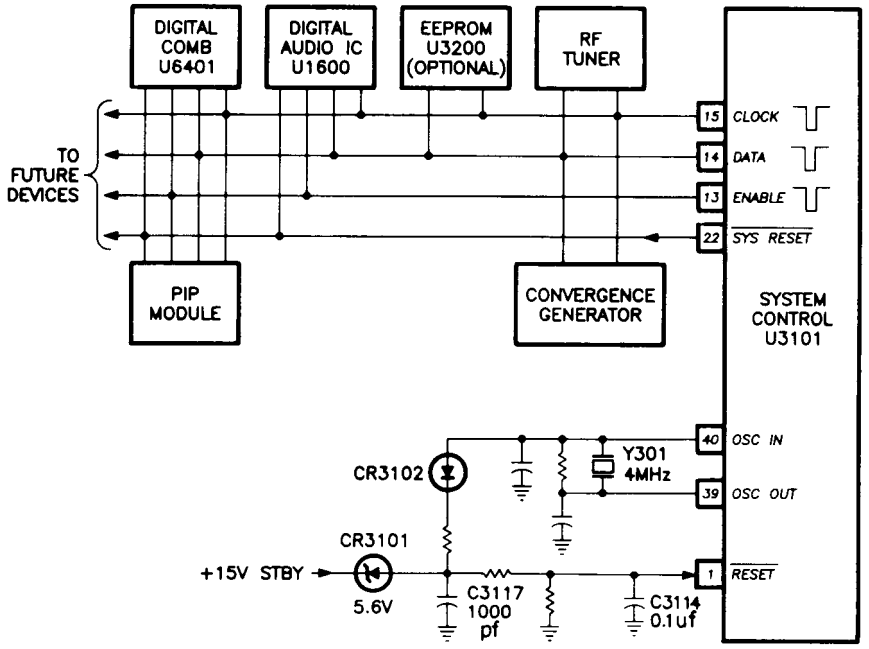

Fig. 6 System Control Serial Bus and Reset

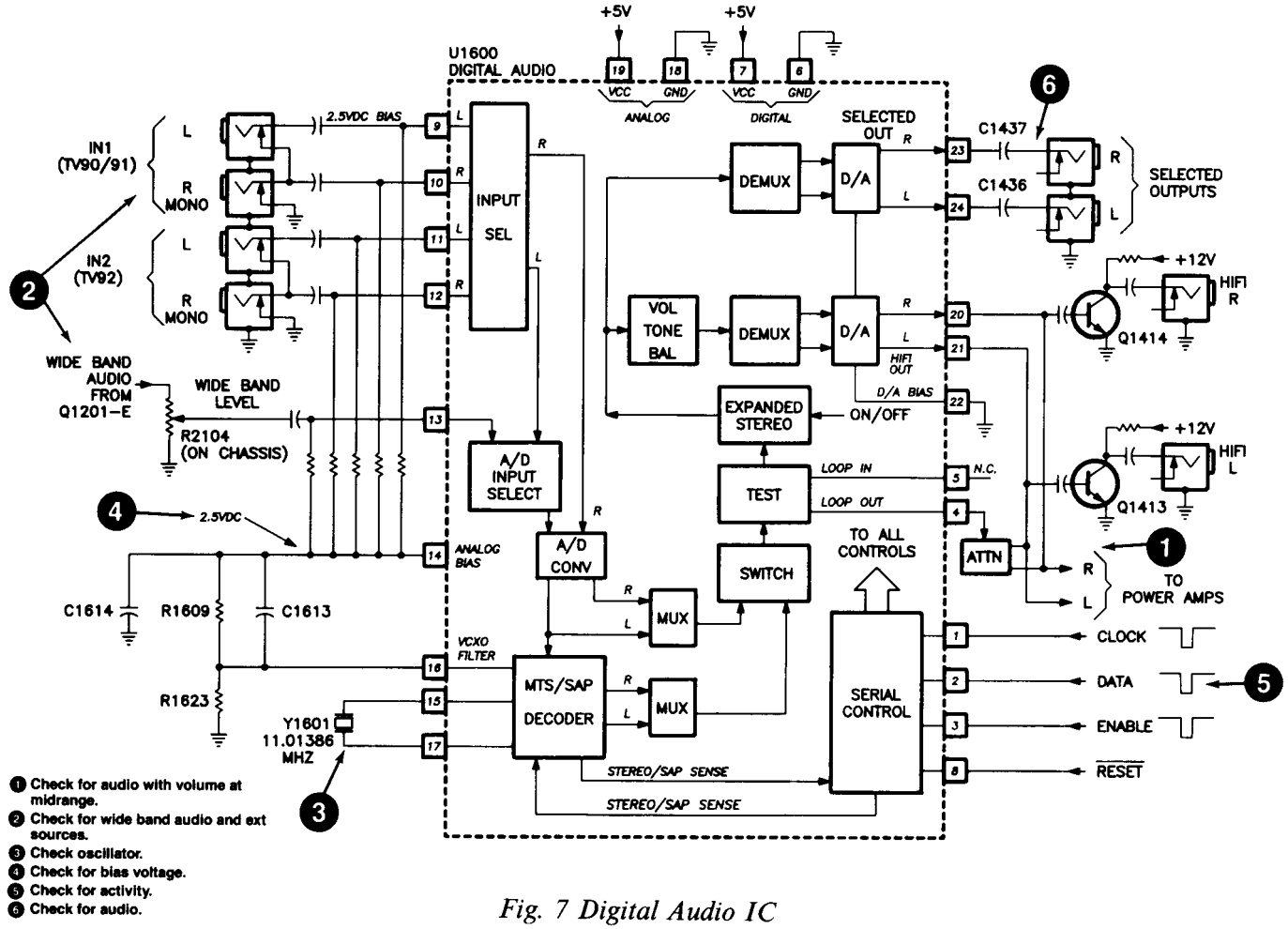

Fig. 7 Digital Audio IC

EXERCISE 3

The set in the tape contains a Pix-in-Pix module. Play the tape and observe and note all the visible symptoms.

_____

_____

QUESTION

1. Having observed the symptoms, what should you do first to determine where the problem lies.

   _____a. Check system control inputs and outputs.

   _____b. Bypass the PIP module to see if it is causing the problem.

   _____c. Check tuner module inputs and outputs.

   _____d. Check luma and chroma going to the one chip.

Watch the tape until the next question.

QUESTION

2. The most obvious conclusion one might make from watching the tape is that the PIP module is defective. What do you think?

   _____a. Yes, the pip module is defective because video returned to normal. Im going to order a new PIP module.

   _____b. The PIP module did cause the video problem and might be defective. I should fix the audio problem before I make a conclusion.

3. What key signals should be checked at the audio IC. (Fig. 7)

   _____a. The audio inputs and outputs of the IC.

   _____b. The master oscillator on the IC.

   _____c. Clock, data, enable, and system reset going to the IC.

   _____d. All of the above.

Watch the tape until the next question.

QUESTION

4. Having repaired the audio problem, our PIP module was reinserted in the set and everything is working normally. How could this be explained?

   _____a. The PIP micro was locked up and being unplugged cleared the problem.

   _____b. The short on the system reset line also kept the PIP micro in reset, preventing it from being initialized by the system control micro.

   _____c. An intermittent connection to the PIP module.

   _____d. Who cares? So what if the customer has to pay for a pip module that didn't need replacing in the first place.

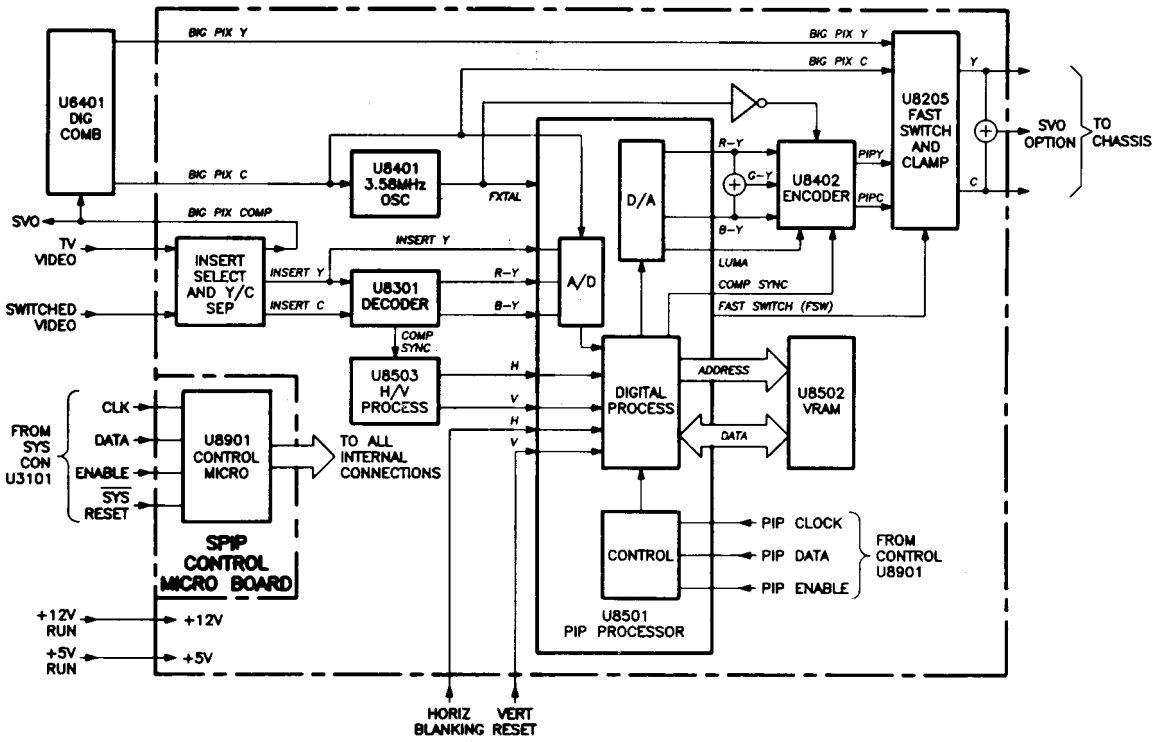

Fig. 8 SPIP Module Block Diagram

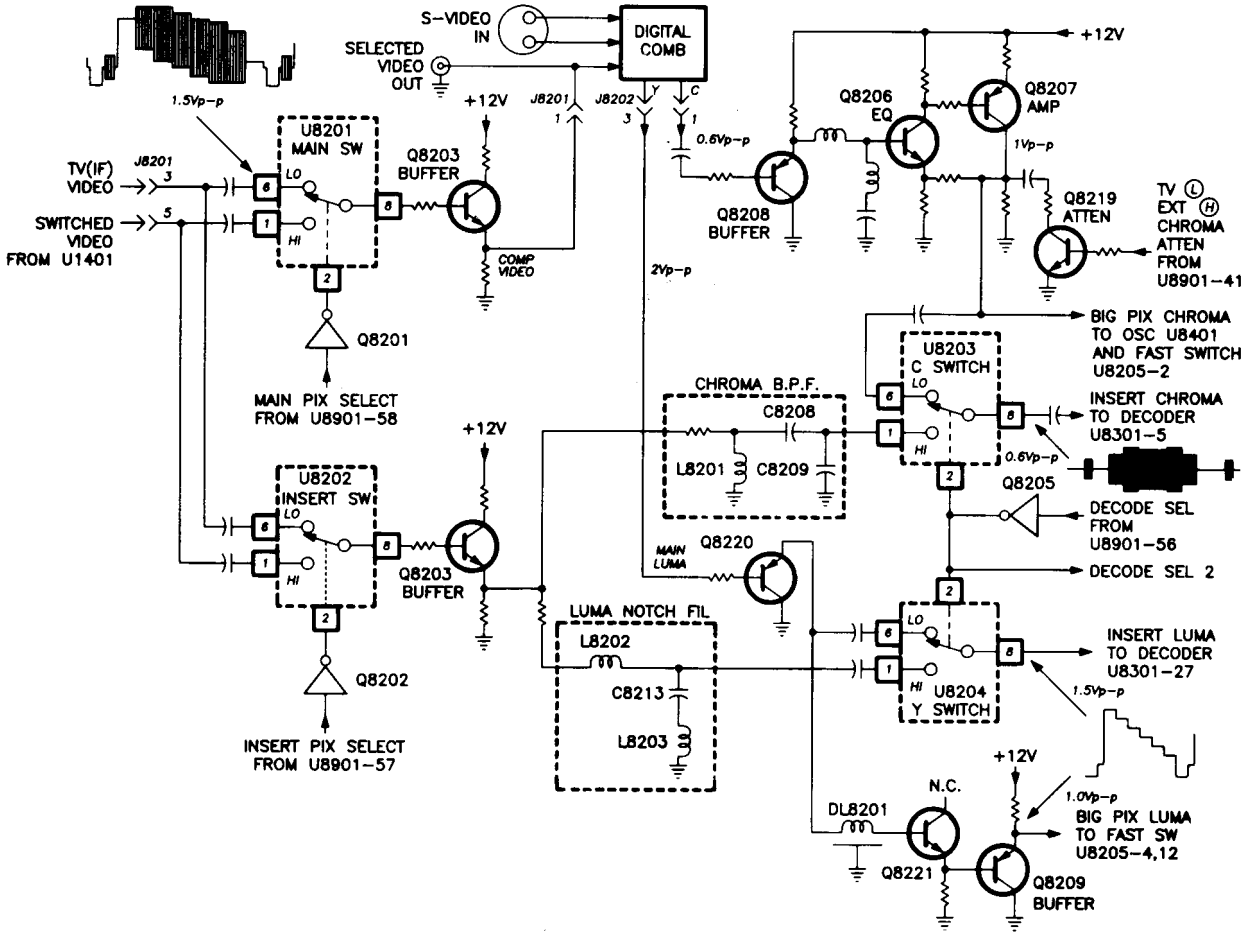

Fig. 9 Input Selection Circuit (SPIP)

EXERCISE 4

Play the tape and observe and note all the visible PIP symptoms.

_____

_____

_____

QUESTION

1. Knowing that the problem lies within the PIP module, refer to the PIP block diagram to determine which circuit area to start troubleshooting.

   _____a. Control Micro U8901.

   _____b. PIP Processor U8501.

   _____c. Input Selection and Y/C Separation.

   _____d. U8402 Encoder.

2. Where would be the best place to check for the video signals that are used to by the pip processor to create the small pix? (Fig. 9)

   _____a. The comb filter on the TV chassis.

   _____b. The Chroma band pass and Luma notch filter.

   _____c. The output of switch U8203 and U8204.

   _____d. The output of switches U8201 and U8202.

Play the tape until the next question.

QUESTION

3. Having fixed the previous problem, you notice small pix sync instability. Which circuit area would you suspect is causing the problem? (Fig. 8)

   _____

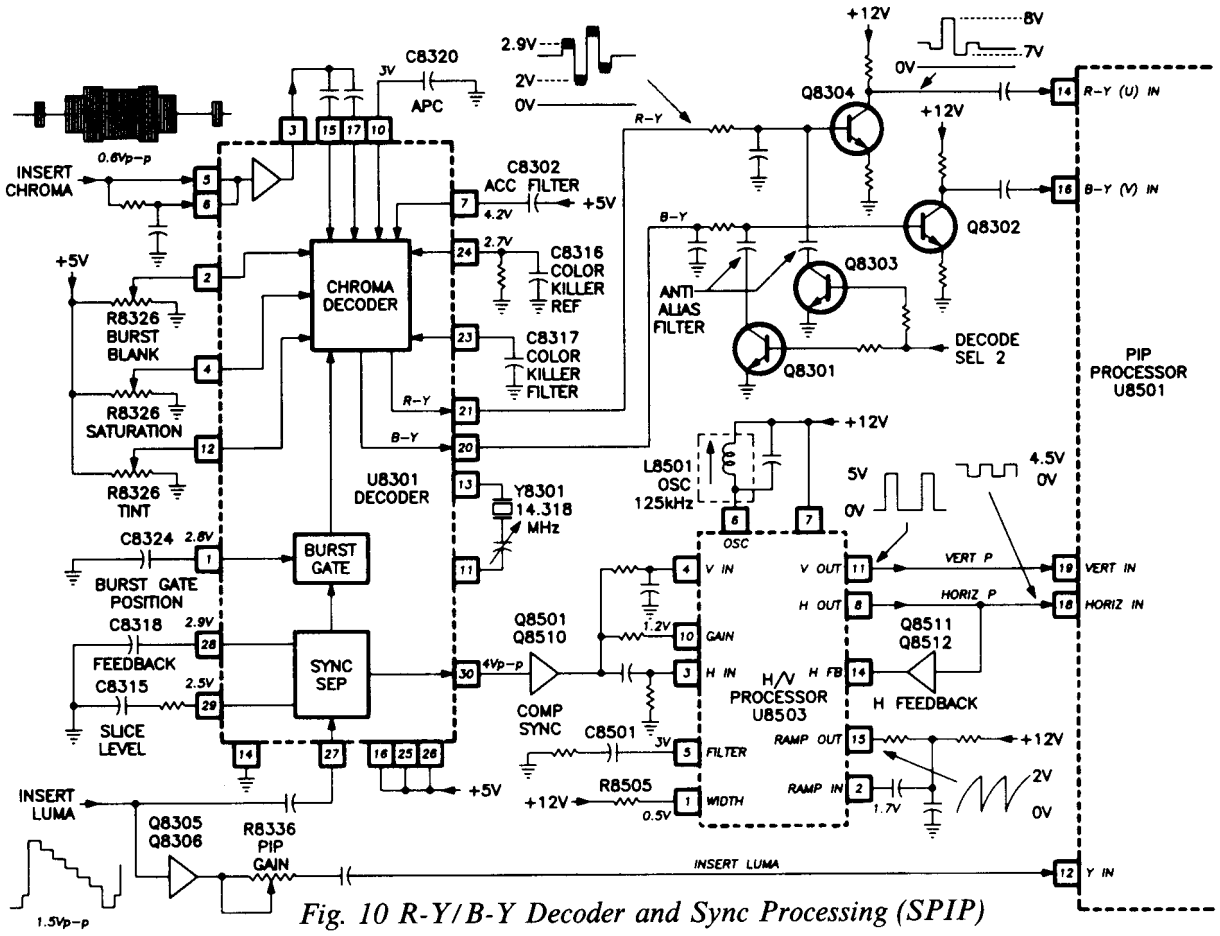

Fig. 10 R-Y/B-Y Decoder and Sync Processing (SPIP)

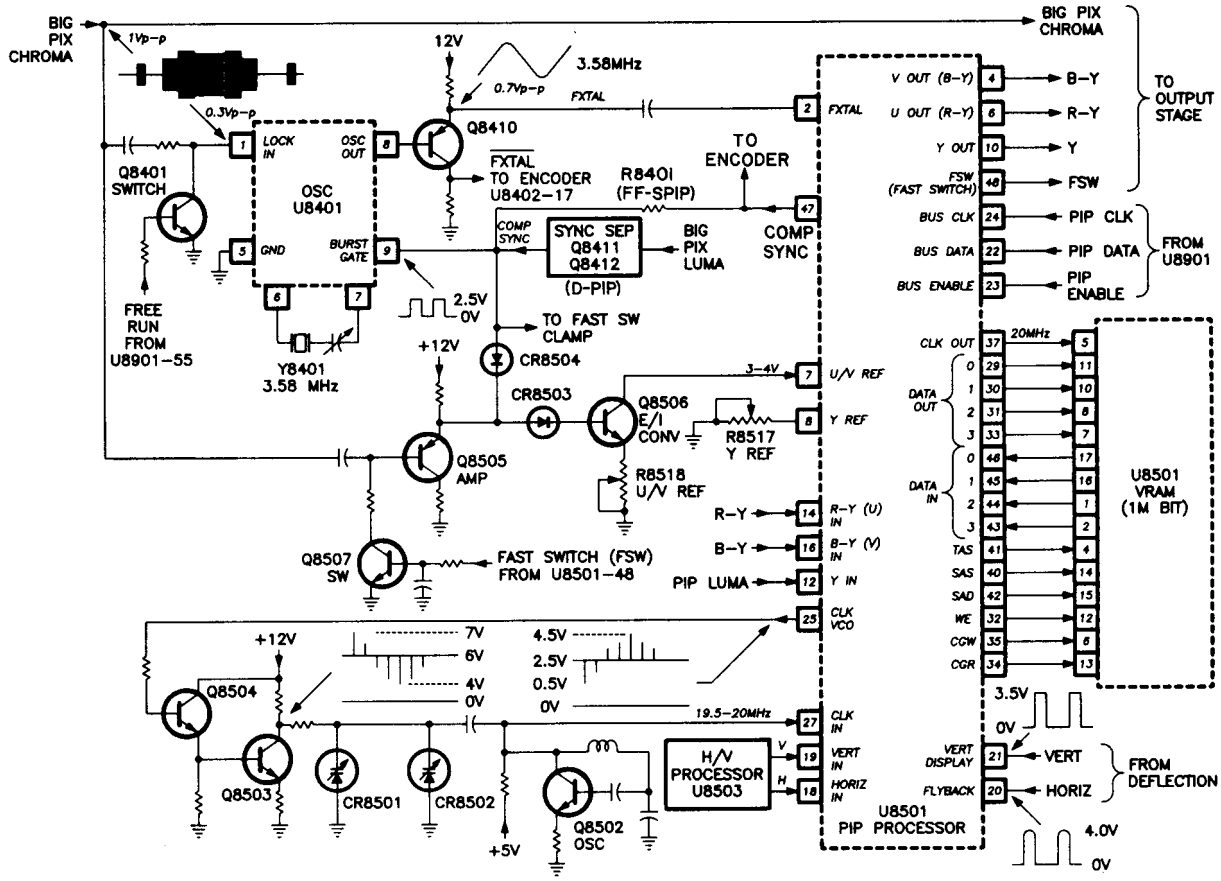

Fig. 11 PIP Processor

4. Which signals in this stage could cause such a symptom? (Fig. 10)

_____a. Loss of sync at H and V inputs to PIP processor.

_____b. No composite sync at U8301-30.

_____c. No insert luma at U8301-27.

_____d. Misadjusted L8501 on U8503-1

_____e. All of the above.

Watch the tape until the next question.

QUESTION

5. Which cirucit area would you suspect for a small pix chroma problem?

_____

6. Which areas in this stage could cause such a symptom? (Fig. 10)

_____a. Loss of Insert Chroma at U8301-5.

_____b. APC, ACC, and Color Killer Ref and Filter.

_____c. Defective U8301.

_____d. Loss of R-Y and B-Y signals to PIP processor.

Watch the tape until the next question.

QUESTION

7. Which cirucit area would you suspect for a distorted small pix problem?

_____

8. Which areas in this stage could cause such a symptom? (Fig. 11)

_____a. Loss of FXTAL signal at pin 2 of PIP Processor.

_____b. Loss of H and V sync signals to PIP Processor

_____c. VCO at PIP Processor.

_____d. VRAM.

9. What is the best way to troubleshoot this stage.

_____a. Decode data lines with logic analyzer.

_____b. Verify activity on all lines between the VRAM and PIP Processor.

_____c. Replace the PIP Processor and VRAM.

Watch to the end of tape.

End of Exercise 4

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